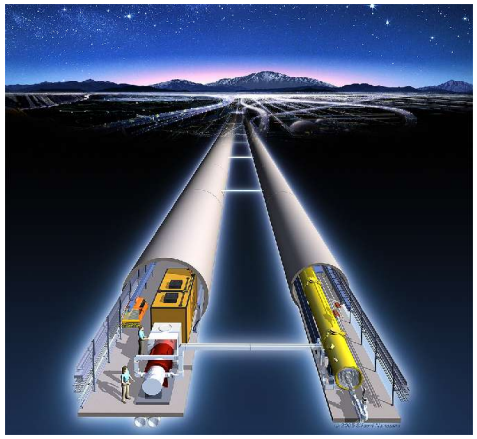
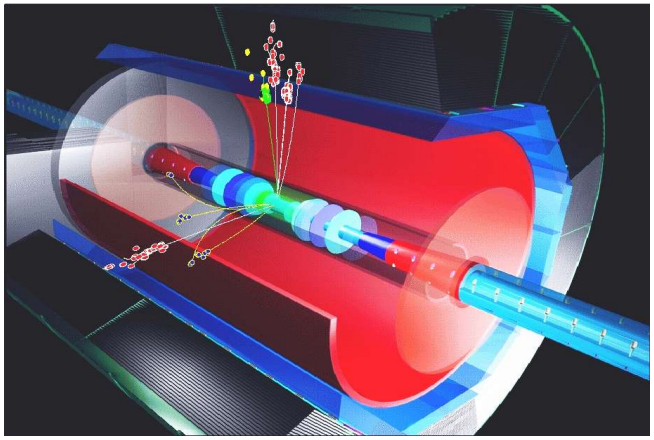
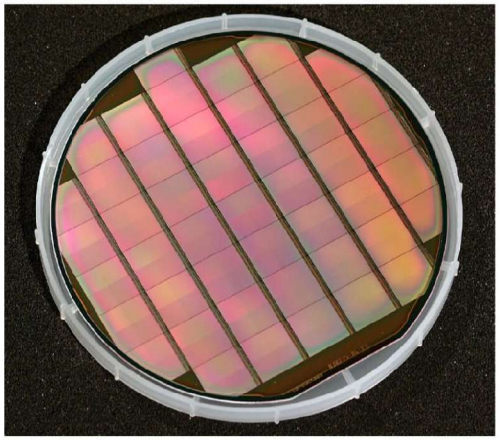
Monolithic Active Pixel Sensors for the Vertex Detector at the International Linear Collider

Warsaw University, 18 May 2005

Devis Contarato

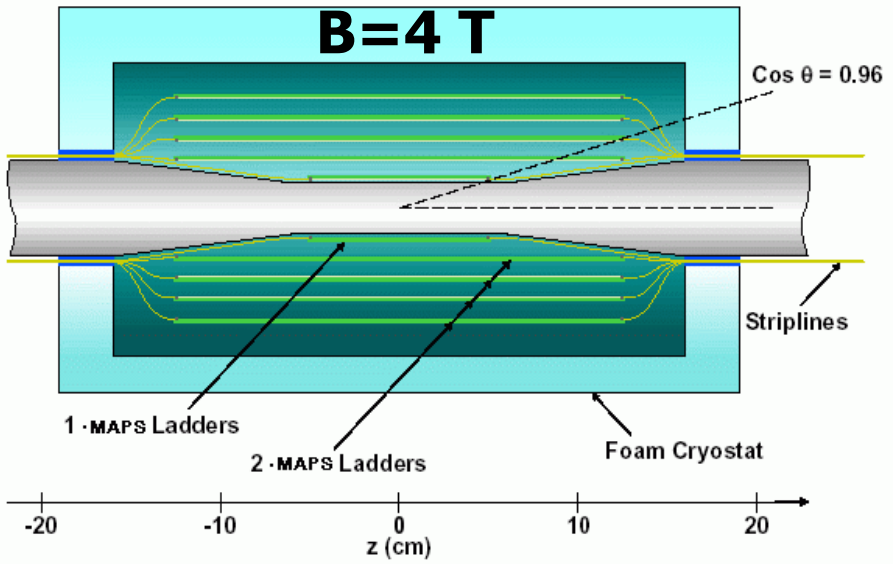
DESY/Hamburg University

Outline

- Introduction: VXD requirements at the ILC
- Features and achievements of MAPS
- Activities of the DESY/Uni-Hamburg group
- Charge collection simulations
- Chip tests: ^{55}Fe, beam-tests, irradiation
- Power dissipation and cooling studies
- Conclusions & Outlook

Introduction: VXD requirements @ ILC

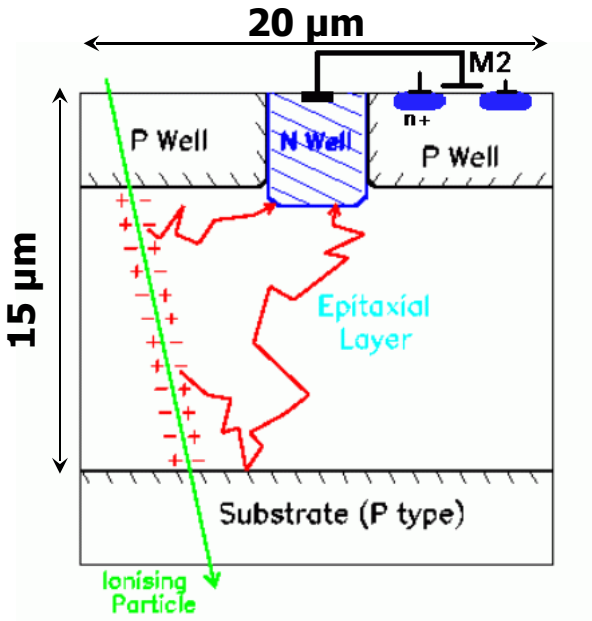
- **High impact parameter resolution**
  - →spatial resolution<5 μm
  - →multiple scattering<0.1% X_0
  - →thin layers ~25-50 μm
- **High granularity** (high jets multiplicity)
  - →pixel pitch of ~20x20 μm^2
- **High occupancy** (e^+e^- pairs background)
  - →fast read-out
  - →on-line data sparsification
- **Harsh radiation environment**:
  - → $\Phi_{neutron} \approx 10^{10}\ n_{(1\ MeV)}/cm^2/year$
  - → $D_{ionisation} \approx 50$ kRad/year

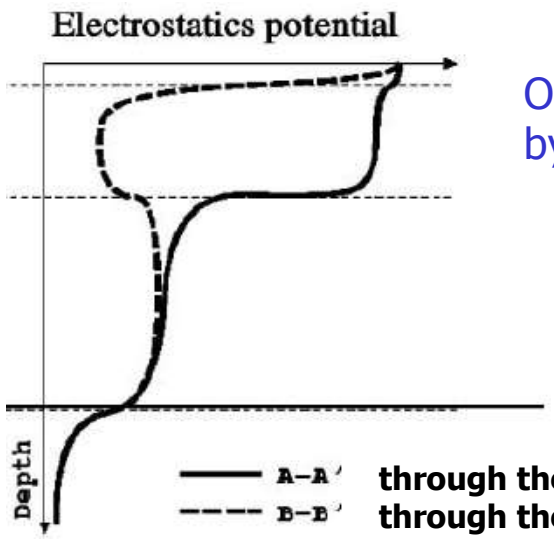


The vertex technology needs to combine high granularity, little multiple scattering, high read-out speed and radiation hardness:

→ natural choice: (thin) pixel detectors

Principles of operation of MAPS

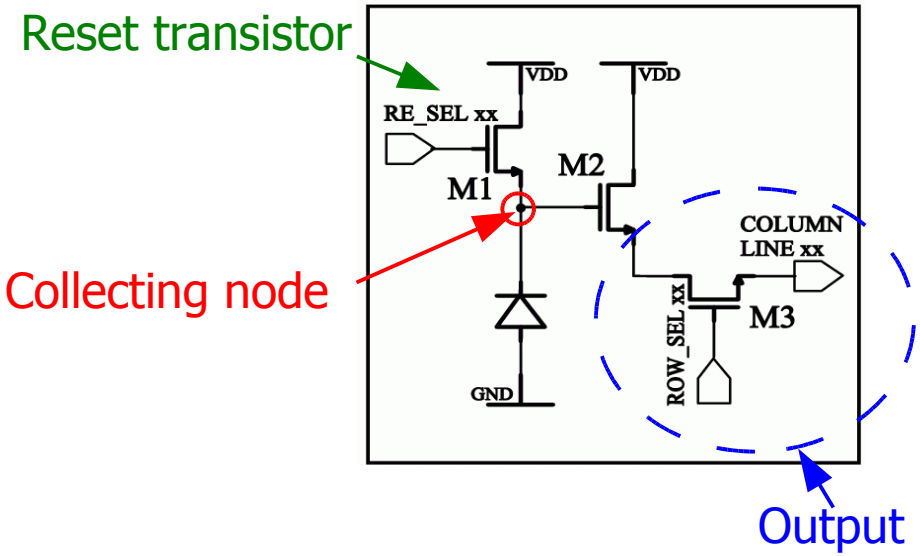




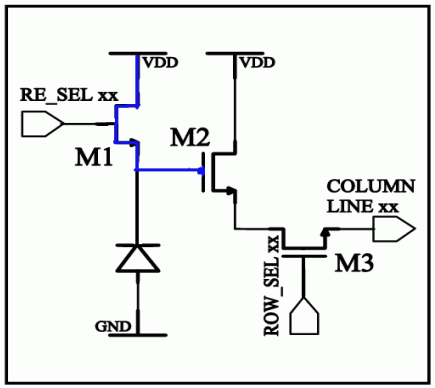
Operational voltage set by CMOS process (no HV)

- **MAPS**: **M**onolithic **A**ctive **P**ixel **S**ensors (a.k.a. CMOS sensors)
- double-well CMOS process with epitaxial layer
- the charge generated by the impinging particle is reflected by the potential barriers due to doping differences and collected by thermal diffusion by the n-well/p-epi diode
- large charge spreading and collection times~100 nsec
- integration of the circuitry electronics on the same sensor substrate

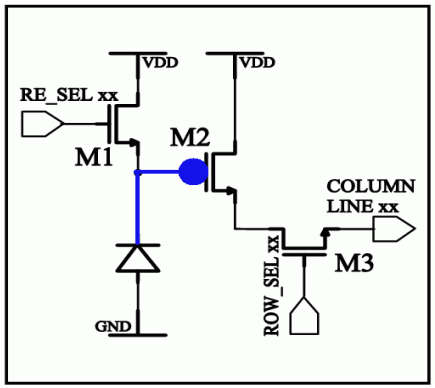
Single pixel read-out



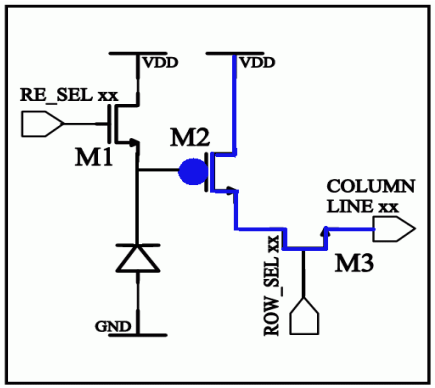
- Classical 3T architecture (3 transistors)
- Other designs possible and also considered
- Single pixel level: reset cycle + integration + readout + reset ...



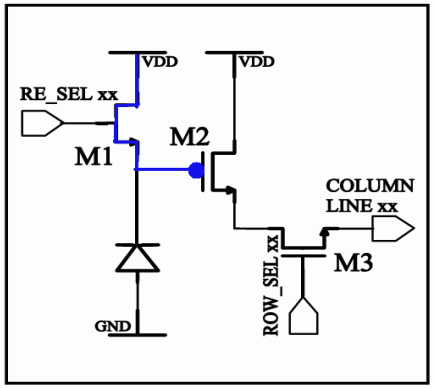
Reset
(common row)



Collection
(int. time=frame rate)

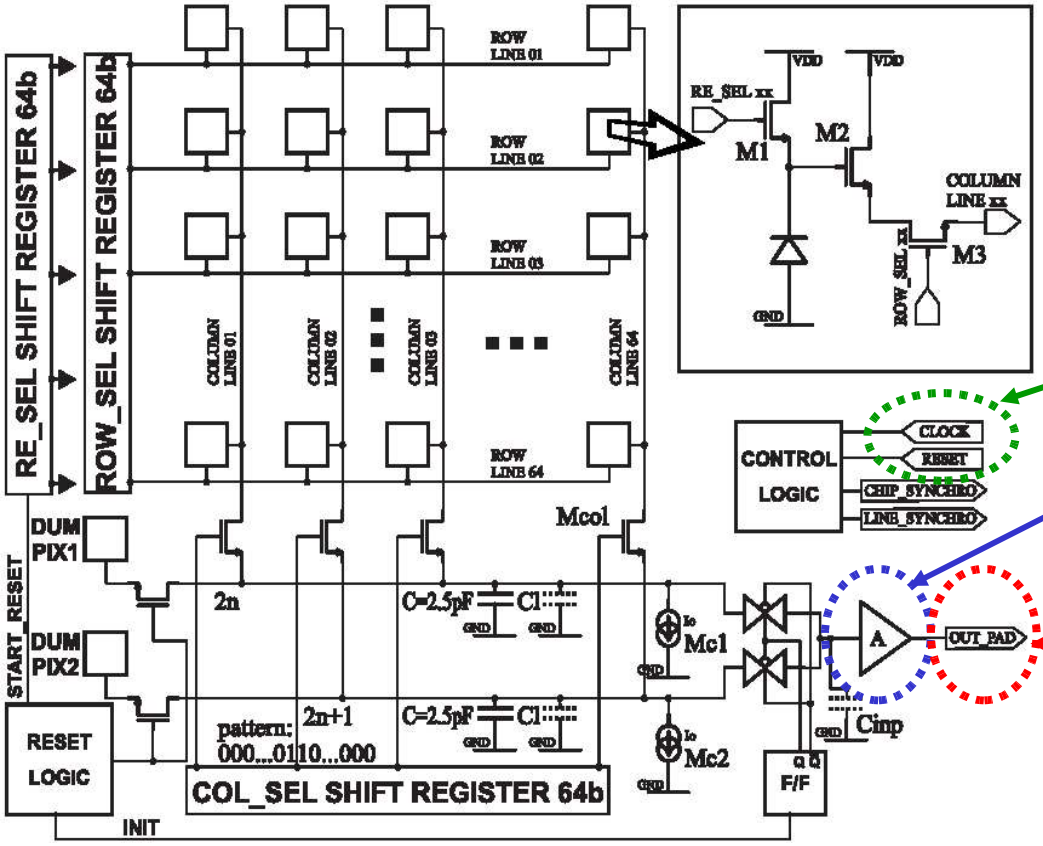


Output



Reset...

MAPS read-out scheme



Prototype maximum clock frequency: 40 MHz

only reset and clock signals needed

last amplification stage common to all

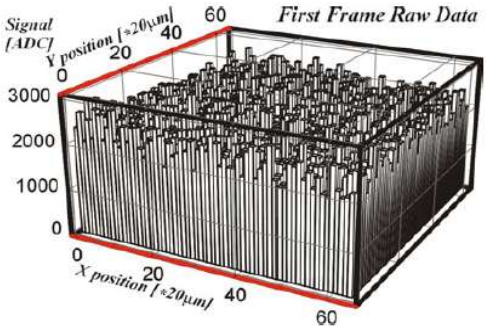
full analog information (all pixels) read-out in series

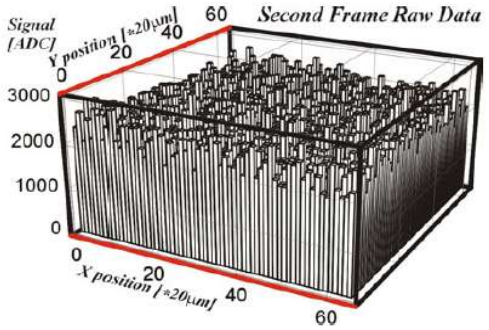
Typical readout scheme for the first prototypes

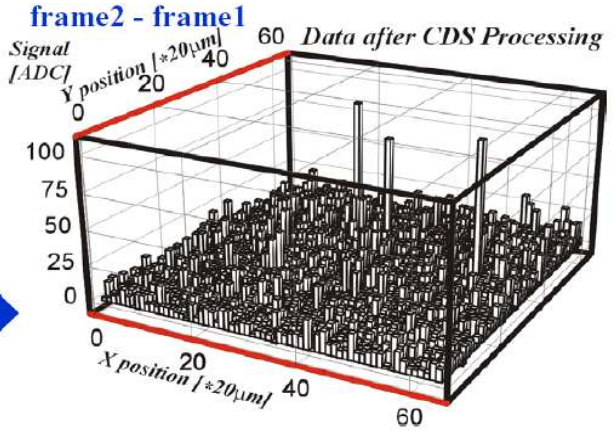
- Reset cycle for all pixel (common row reset) + serial readout
- Cell output is amplified - physical signal: two frames are read-out and subtracted (to subtract noise/pedestals) – Correlated Double Sampling (**CDS**)

Correlated Double Sampling

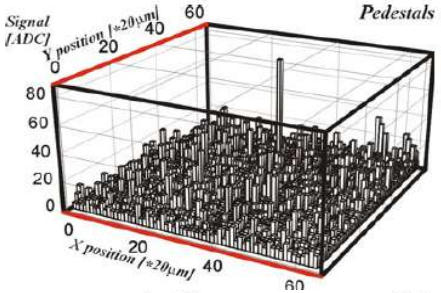
CDS : get rid of FPN, reset noise, 1/f noise



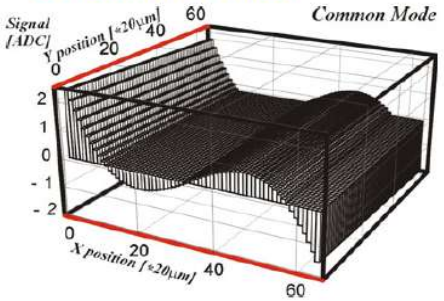


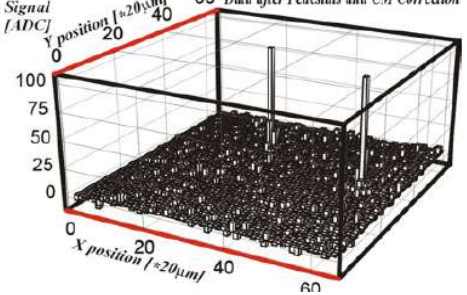


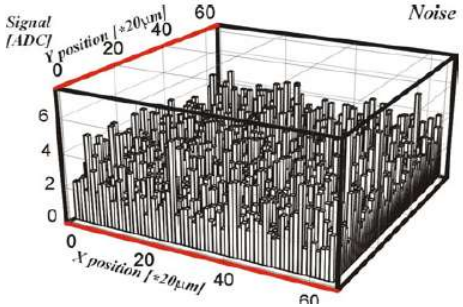
- **CDS Pedestals:**



- **Common Mode:**

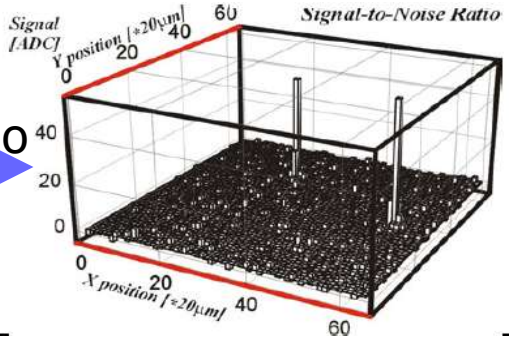






Signal/Noise ratio

for given event



Why MAPS as the technology for the VXD?

- Integration of signal processing electronics on the same sensor substrate → system-on-chip
- Thin sensitive volume and possibility of thinning down → low material budget
- High granularity → good spatial resolution
- Improved read-out speed (e.g. column-parallel readout)
- Radiation tolerance
- Use of standard CMOS technology → large scale availability at low cost

History of MAPS prototypes

MIMOSA = **M**inimum **I**onising **MOS** **A**ctive pixel sensor

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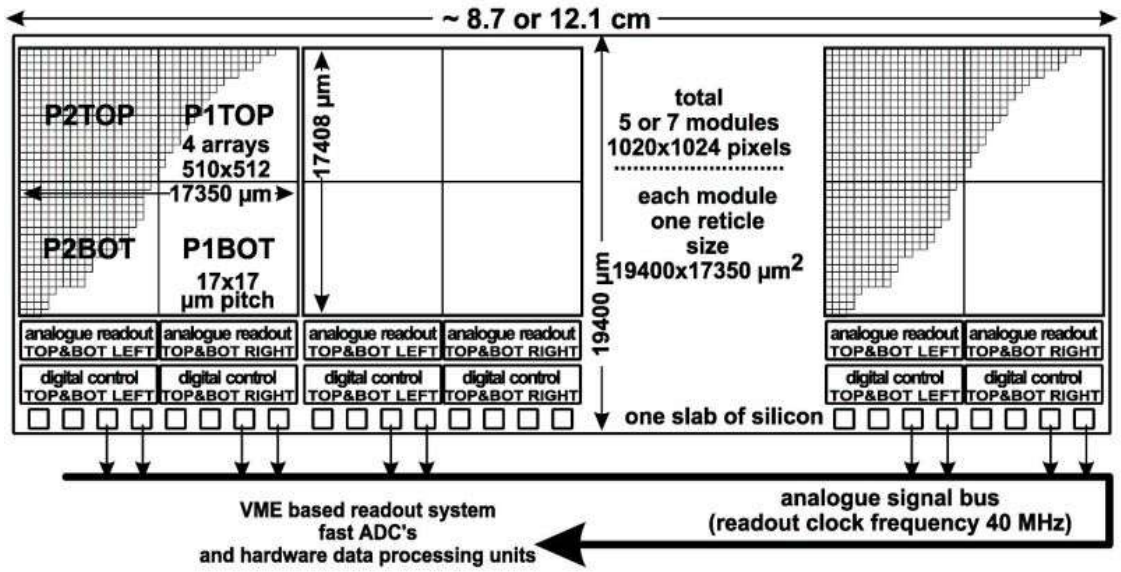
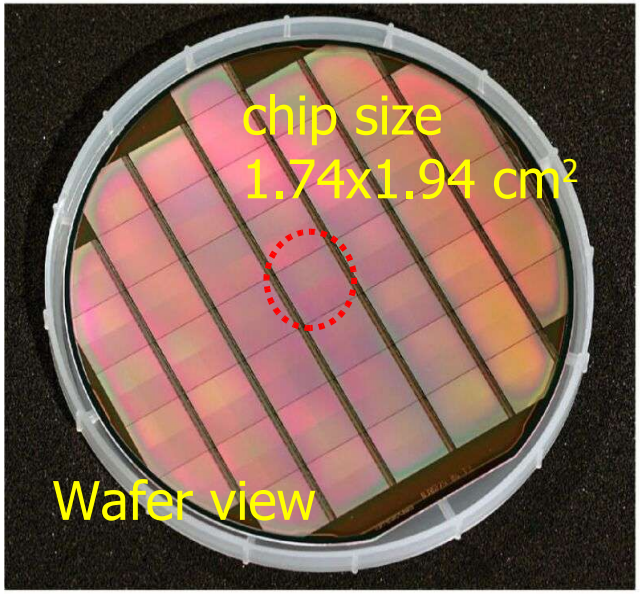
Prototype	Process	Epi-thickness [μm]	Pixel pitch [μm]	Features
MIMOSA 1	AMS 0.6 μm	14	20	Thick epitaxy, technology demonstration
MIMOSA 2	MIETEC 0.35 μm	4.2	20	Thin epitaxy
MIMOSA 3	IBM 0.25 μm	2	8	Deep-submicron process, rad. tol. design
MIMOSA 4	AMS 0.35 μm	0	20	No epitaxy, low-doping substrate
MIMOSA 5	AMS 0.6 μm	14	17	1 Mpixel real-size sensors
MIMOSA 6	MIETEC 0.35 μm	4.2	28	Column-parallel read-out, integrated sparsification
MIMOSA 7	AMS 0.35 μm	0	25	Column parallel r.o. + integr. sparsification (photoFET)
MIMOSA 8	TSMC 0.25 μm	8	25	Column-parallel read-out, integrated sparsification
MIMOSA 9	AMS 0.35 μm	20	20/30/40	Technology tests, different parameters (pitch)
MIMO*	TSMC 0.25 μm	8	30	STAR VXD upgrade
MIMOSA 11	AMS 0.35 μm	20	20	Radiation hardness studies

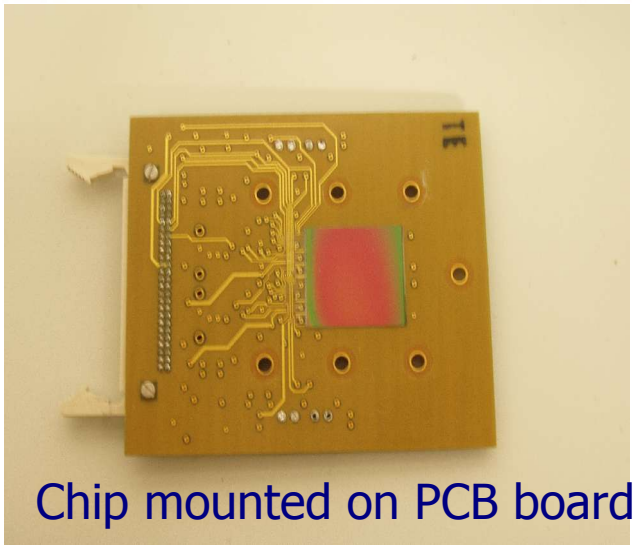
...and more to come: submission of M12/M13 under way

MIMOSA V: real-size prototype



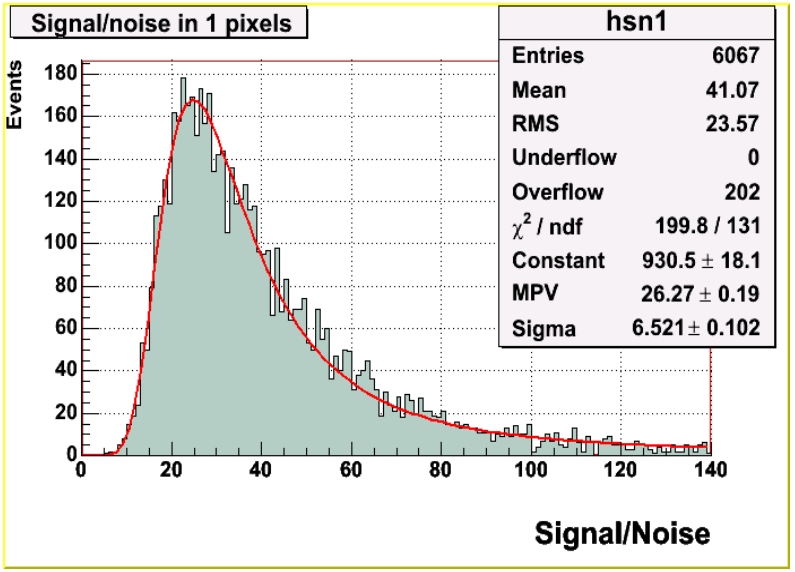


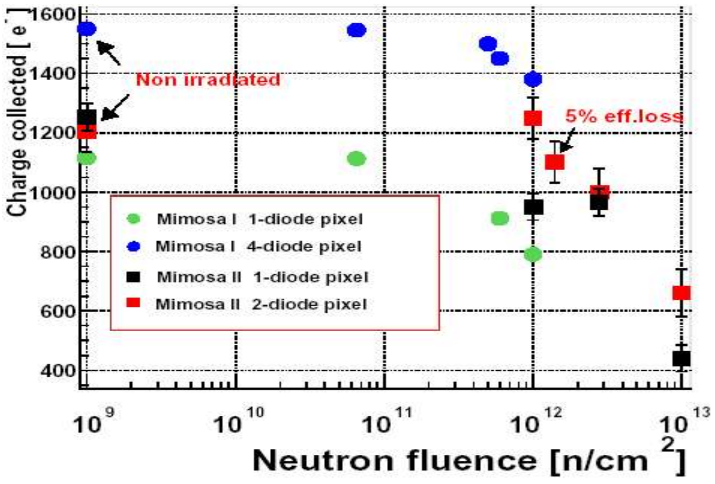
- Real-size prototype: 3.5 cm², 1M pixels
- First ladder concept attempt
- AMS 0.6 µm CMOS with 14 µm epilayer
- pixel pitch 17x17 µm²
- 4 independent matrices of 512x512 pixels
- serial analogue readout @ 10 MHz
- back-thinned down to 120 µm

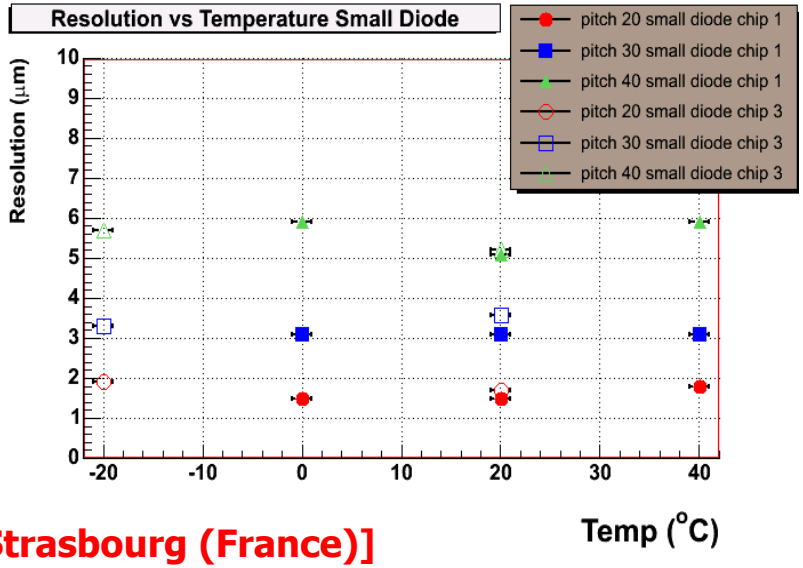


Achievement of MIMOSA sensors

- Several fabrication processes explored
- Tracking performances (100 GeV/c π @ CERN):
  - S/N~20-30
  - noise~10-20 e
  - detection efficiency>99%
  - single point resolution: 1.5-2.5 μm
- Performances reproduced with large size prototype (e.g. imager)
- Radiation tolerance against neutrons and TID asserted within ILC requirements







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DESY/Uni-Hamburg activities on MAPS

- **Detector performance studies**
  - Simulation of charge collection (ISE-TCAD)
  - Test-stand and test-beam measurements (MIMOSA V)
  - Radiation damage and material investigations
- **Mechanical design and cooling**
  - Mechanics: CAD design of VXD layers layout
  - VXD cooling: simulations, material budget, power switching
- **General detector design and optimization**
  - Physics simulation of Vertex Detector

Issues for device simulation (ISE-TCAD)

3-D device physics simulations are performed in order to:

- understand the charge collection mechanism and its time properties
- estimation of the charge collection efficiency
- study of the spatial charge spreading onto neighboring pixels
- study of the influence of technological parameters on the sensor charge collection properties
- optimisation of the sensor design

Overview of ISE-TCAD simulations

Description of boundaries, doping and mesh

MESH GENERATOR

Physical models and parameters

DEVICE PHYSICS SIMULATOR

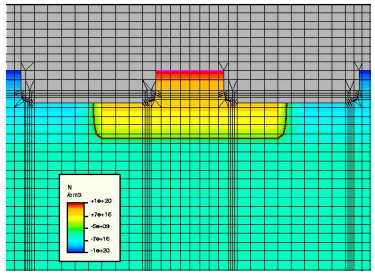
SIMULATION RESULTS

VISUALIZATION TOOLS

Boundaries…

Doping…

Mesh…



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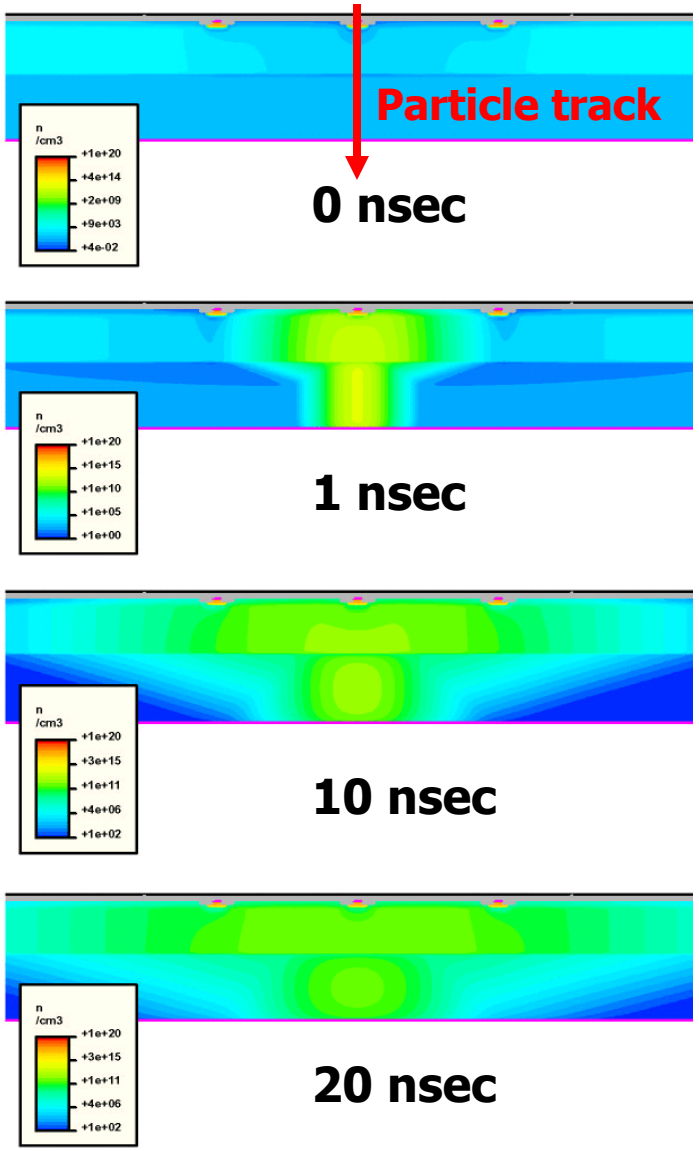
Physics…

Parameters…

Solve…

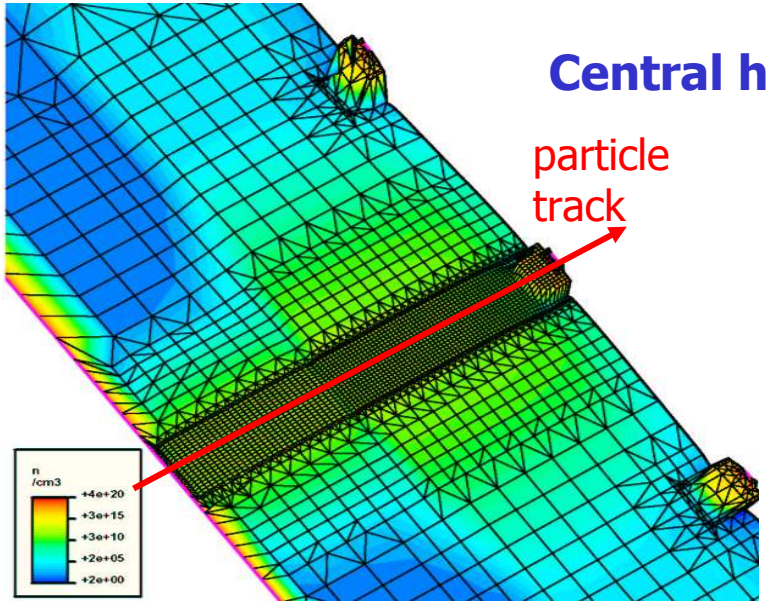
Simulation of charge collection

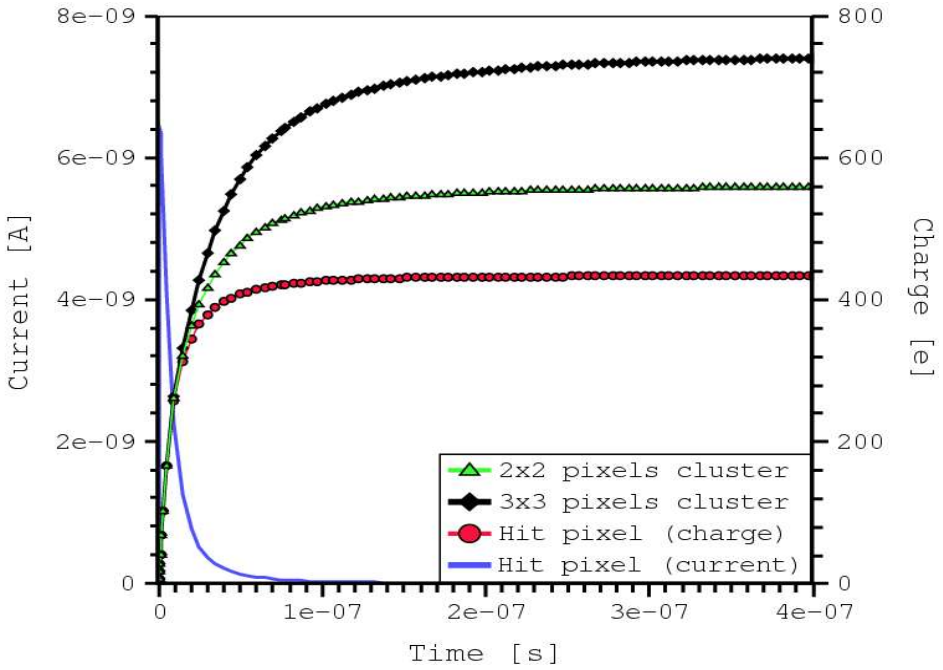
- Simulated structure: 3-dim model of 3x3 pixel cluster (3 pixels in 2-dim)
- Technological details and doping profiles from foundry (approximate)
- The passage of a MIP is simulated introducing an excess charge (80 e-h pairs/μm)
- Transient simulation: relaxation process of achieving equilibrium after the particle passage
- Study of different impact positions for the simulated MIP



MIMOSA V Simulation

Pixel pitch 17 μm, diode 3 μm, EPI-thickness 14 μm, 3x3 pixels cluster



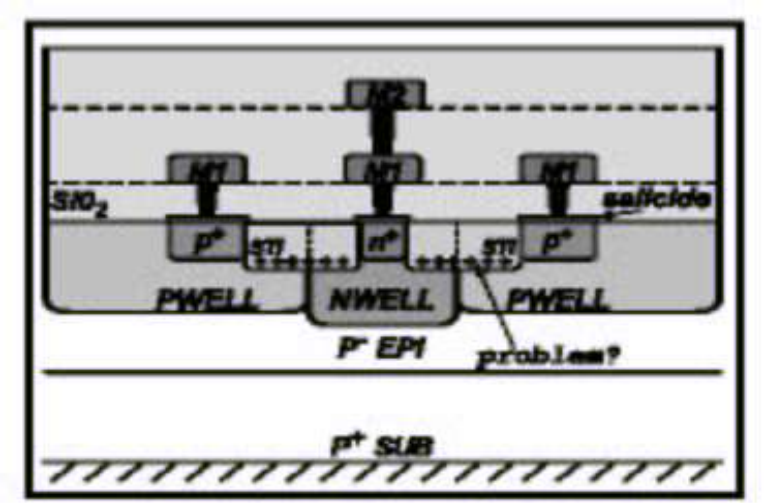


- larger diffusion in the epilayer, fast recombination in the substrate (different carrier lifetimes)
- expected signal ~1000 e: large charge sharing (clustering)
- charge collection times <100 ns

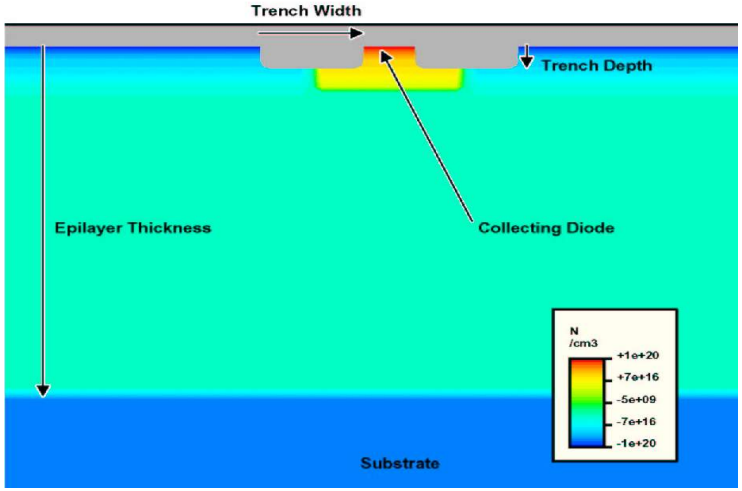
Going to deep-submicron technology

Future: probably only deep-submicron (≤0.25 μm) technology available

- smaller epilayer thickness: smaller signal + substrate contribution to the collected charge
- latch-up of the transistors requires trench isolation
- radiation-induced interface states at the Si/SiO_2 interface



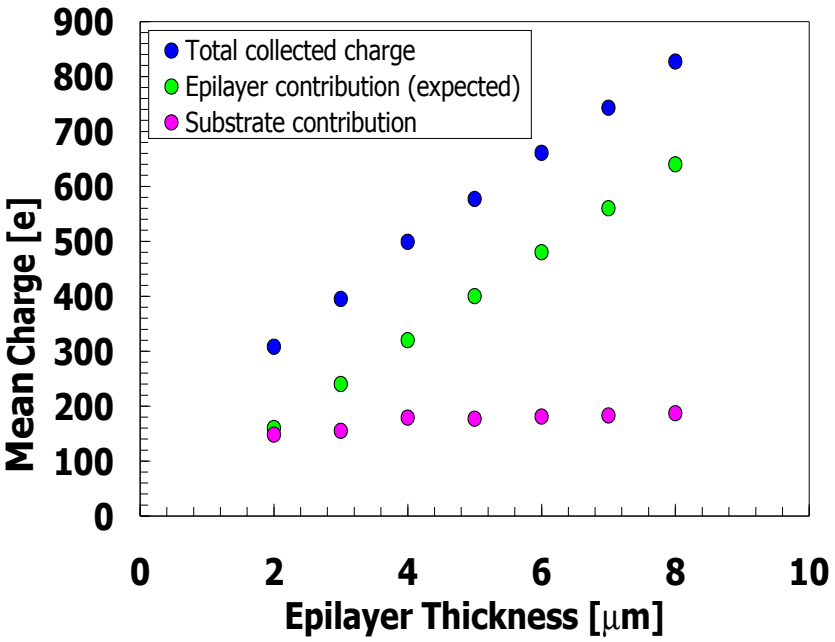
Configuration of the collecting diode in a sub-μm process with Shallow Trench Isolation

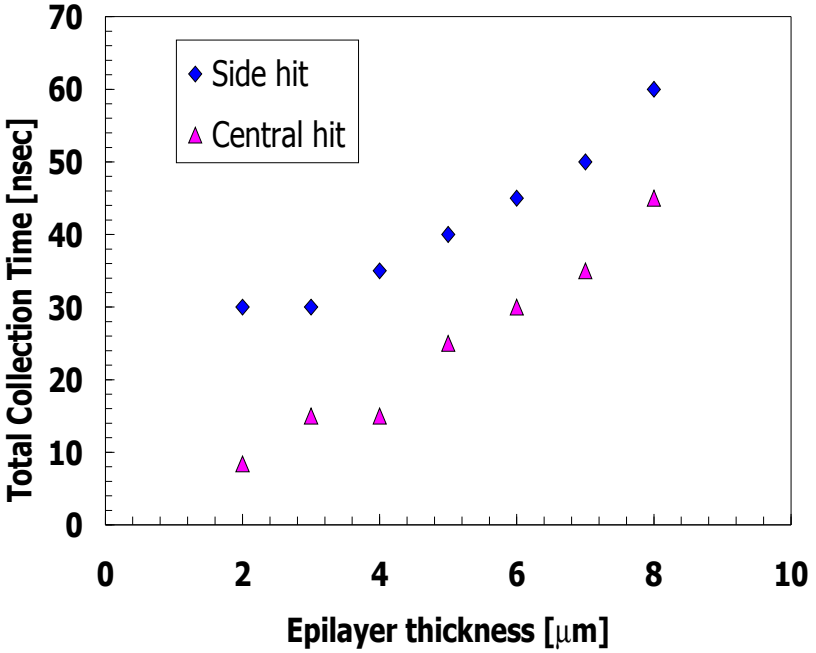


Example of simulated structure and geometrical parameters used in the simulations

Charge collection in deep-submicron MAPS

Pixel pitch 20 μm, diode 1 μm, EPI-thickness 2÷8 μm, typical doping profiles



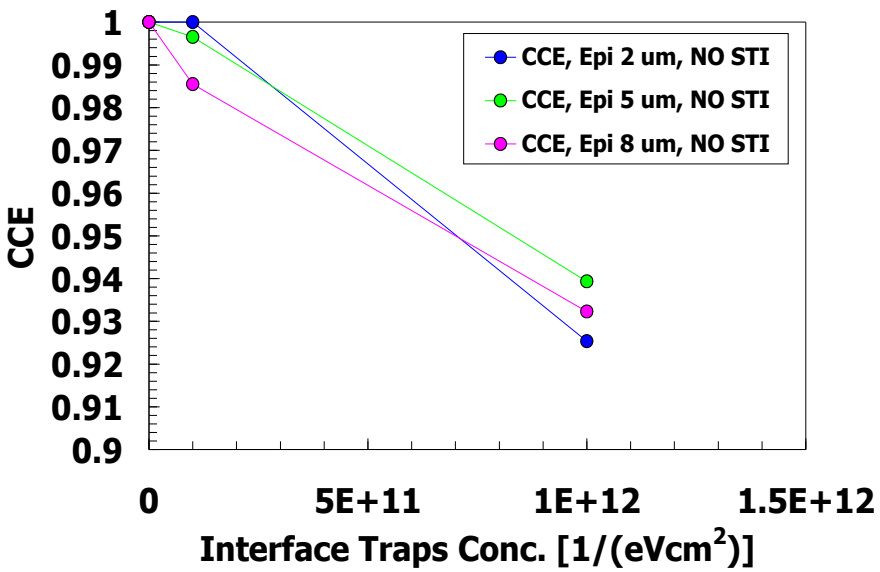


- Linear dependence of collected signal on epilayer thickness
- Important substrate contribution
- A thinner epilayer results in smaller signal, but limited charge spreading and shorter collection times (faster collection)

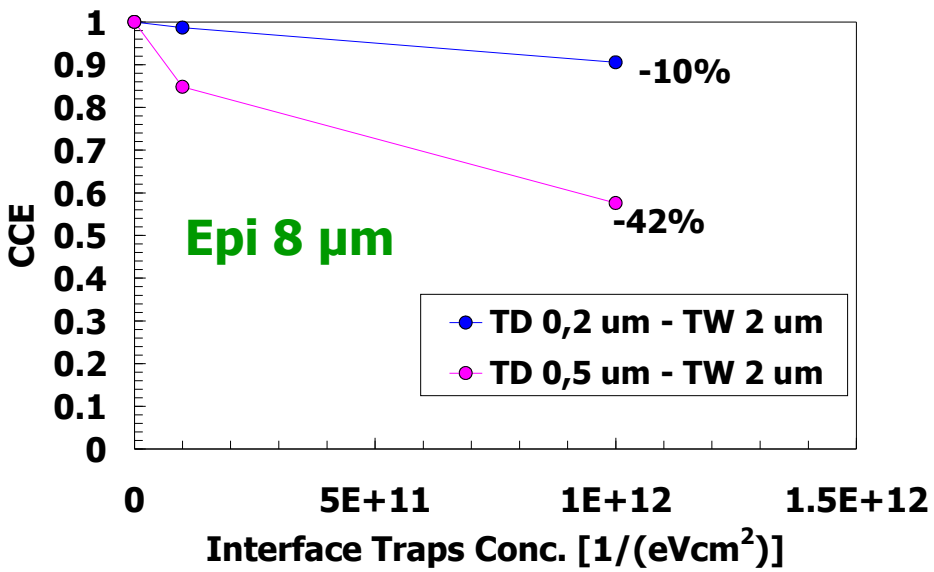
Simulation of interface damage

(Interface traps concentrations: 10^{11}, 10^{12} 1/eVcm^2 ~500 krad, Wüstenfeld 2001, Ph.D. thesis)

No shallow trench isolation



Shallow trench isolation



- Significant dependence of the collected charge on the trench geometry (mainly on depth, less dependence on trench width)
- Collection times are not affected
- How to overcome the problem: PolySi instead of $Si0_2$?

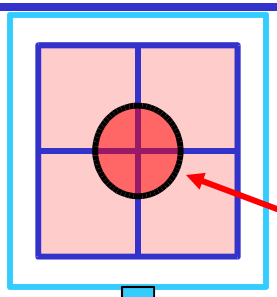
Test stand for chip characterization

- MIMOSA V chip (262K pixels/matrix)
  - clocked with 10 MHz
  - matrix read-out time 26ms
- Cooling unit
- VME-Based readout
  - clock & reset signals
  - ADC board
- Radioactive source tests

^{55}Fe - X rays

- Planned tests:
  - IR laser light injection
  - B-field dependence
  - on/off power switching

Data acquisition system



MIMOSA V chip on front-end board and cooling unit

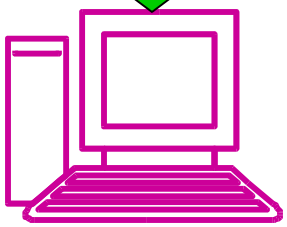
Source

Serial analog output

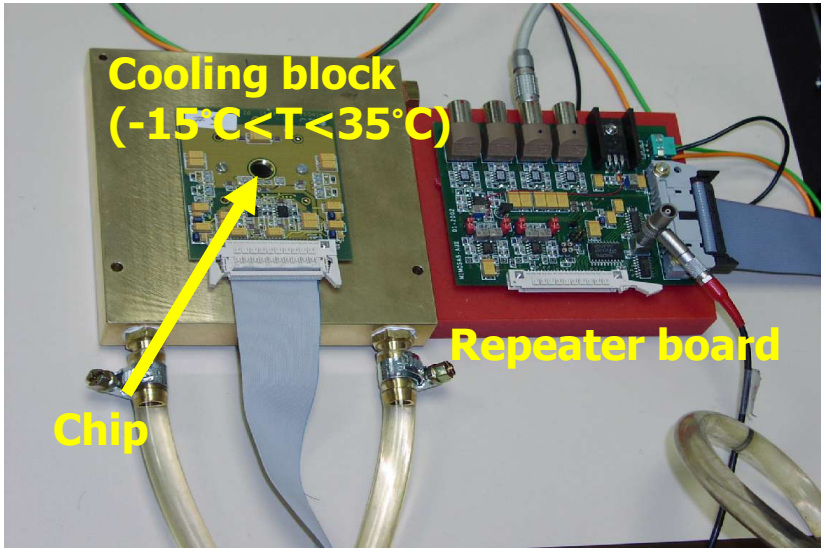
Interface board - Repeater

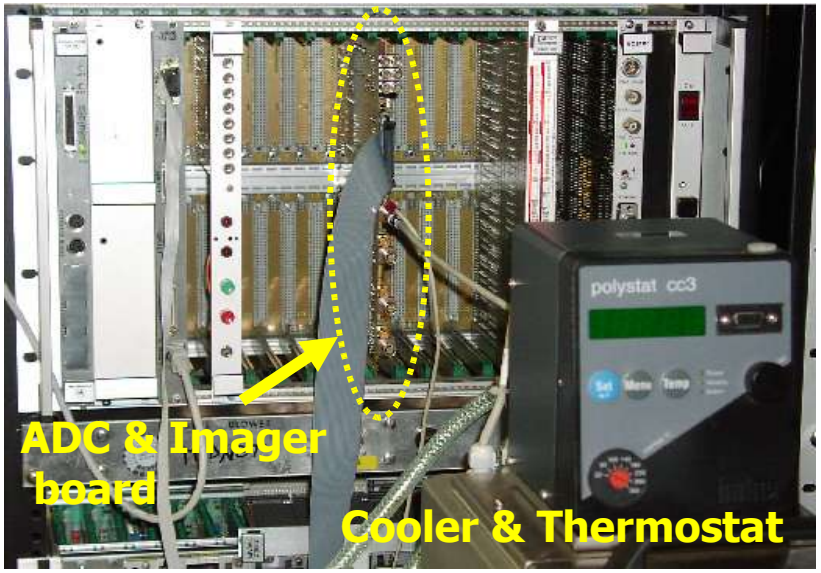
Imager board – VME Flash ADC unit

VME-based read-out system and hardware data processing units

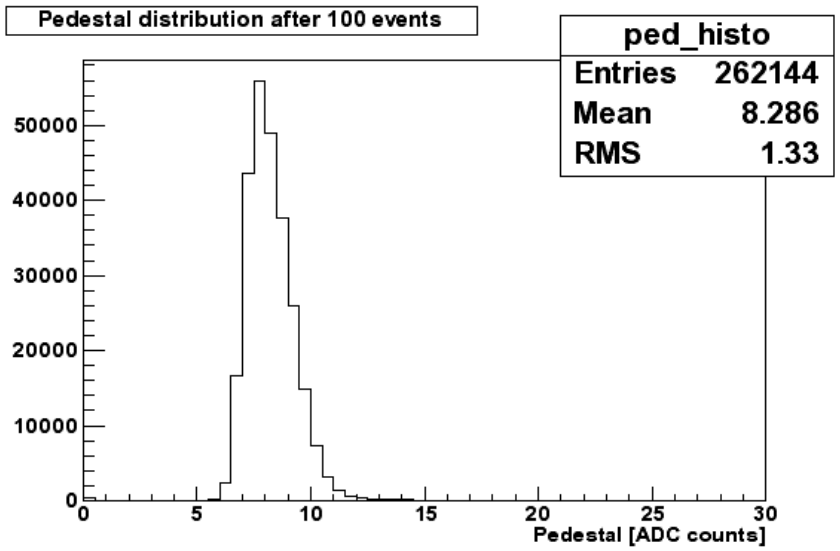


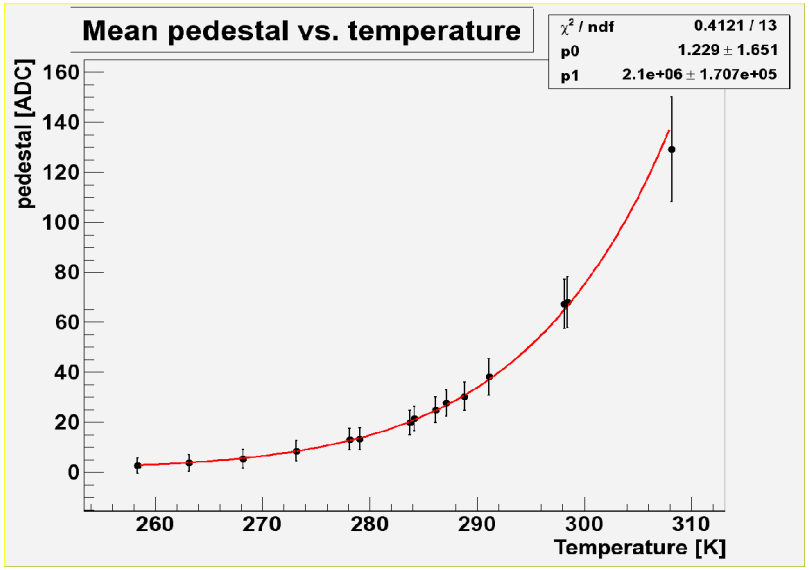
Software for data acquisition and analysis

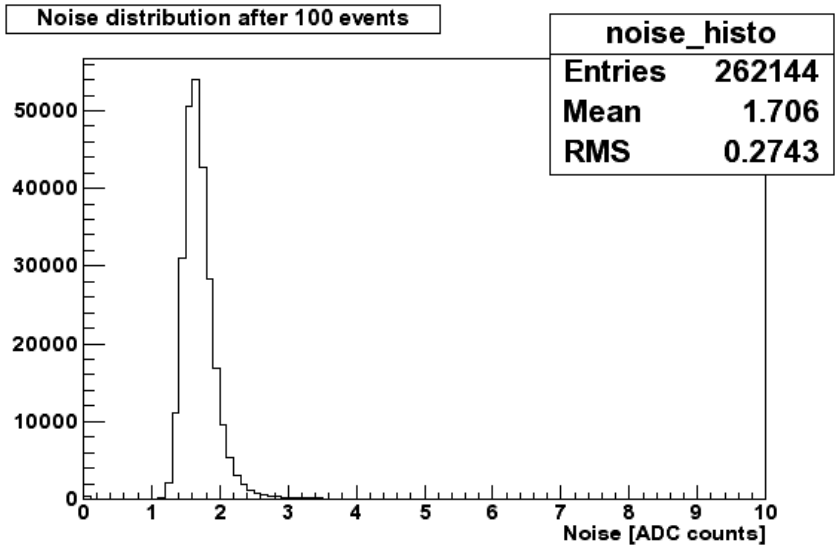




Pedestals and noise







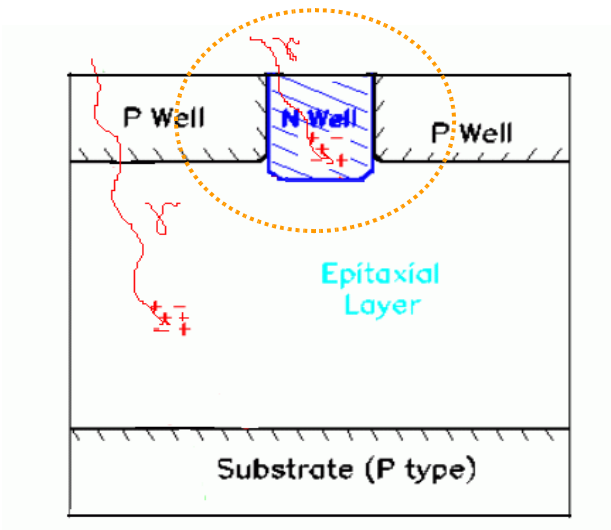
- Pedestal and noise are uniform over all the matrix
- Good agreement with fit function:

$$pedestal = c_0 + c_1 T^2 \exp\left(-\frac{E_g}{2k_B T}\right)$$

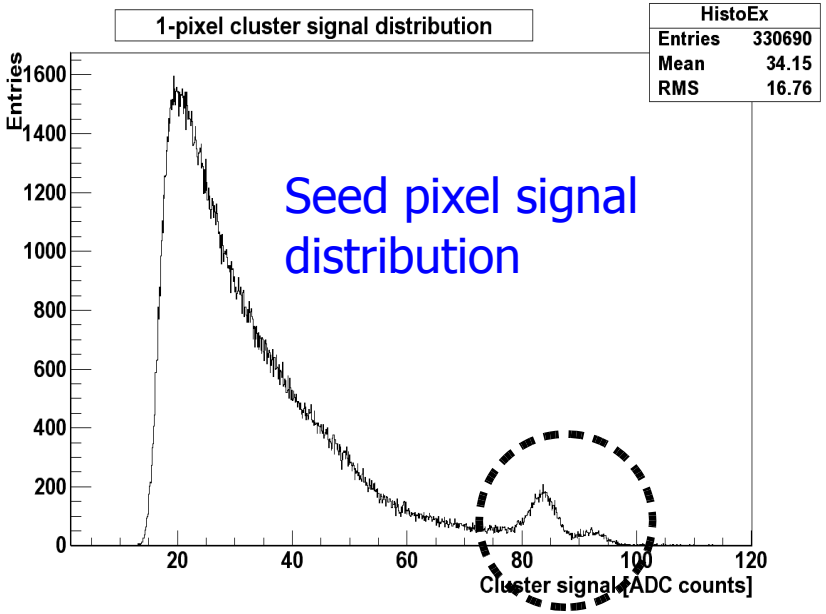
leakage current term

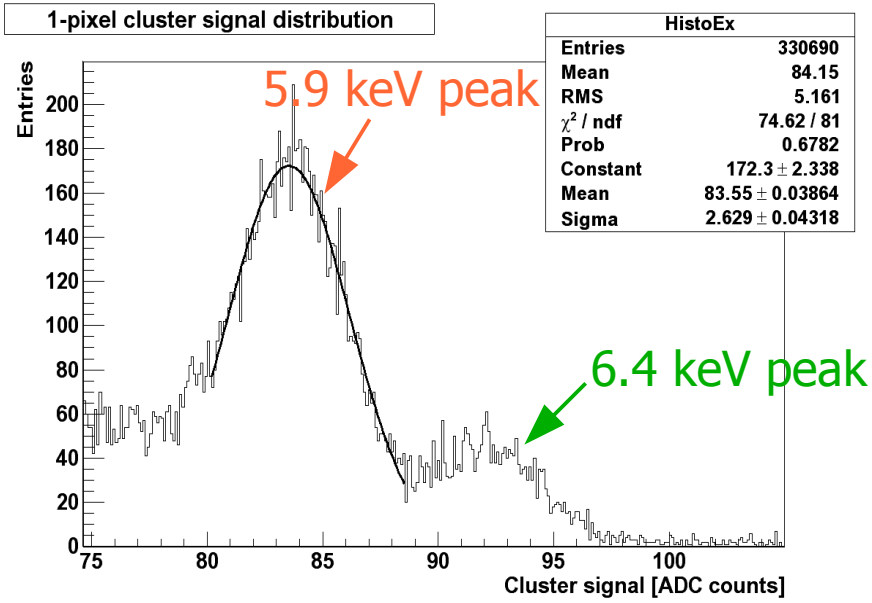
→ pedestals ($\propto I_{leak}$) can be used to measure I_{leak} after irradiation

Calibration with ^{55}Fe

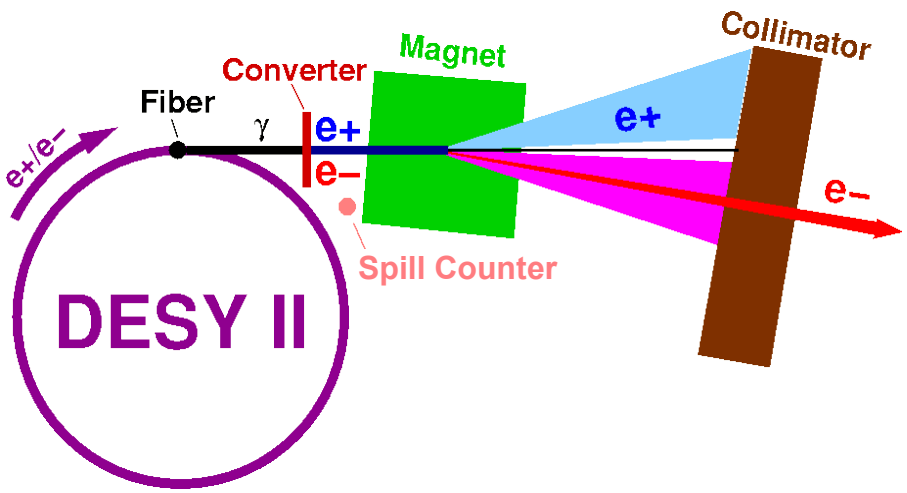


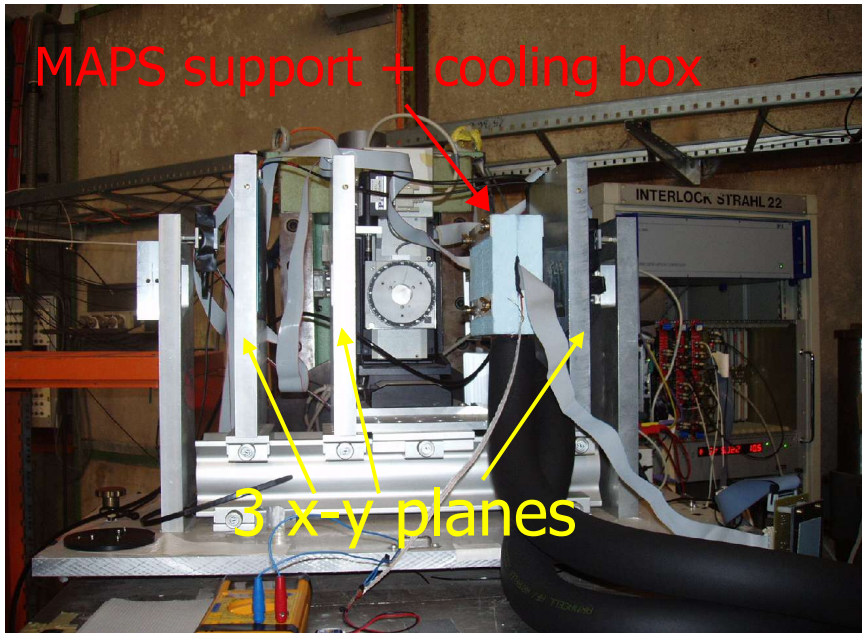
- Looking for conversion of the photons in the n-well (assume 100% charge collection efficiency)
- 5.9 keV photons generate ~1640 e
- Peak used to calibrate e/ADC conversion and noise
- ENC~20 electrons





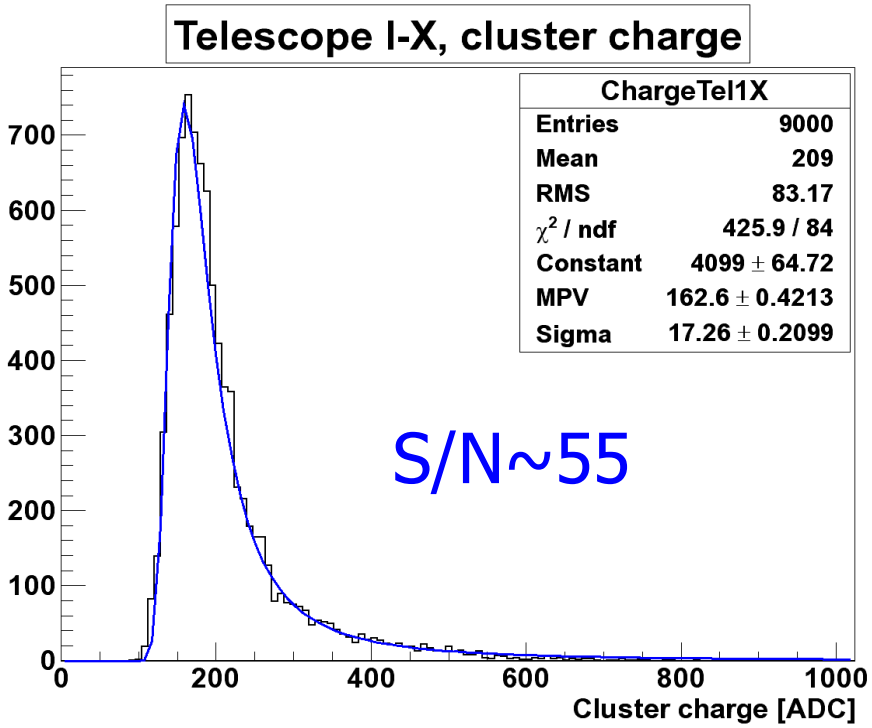
Beam-tests at DESY II

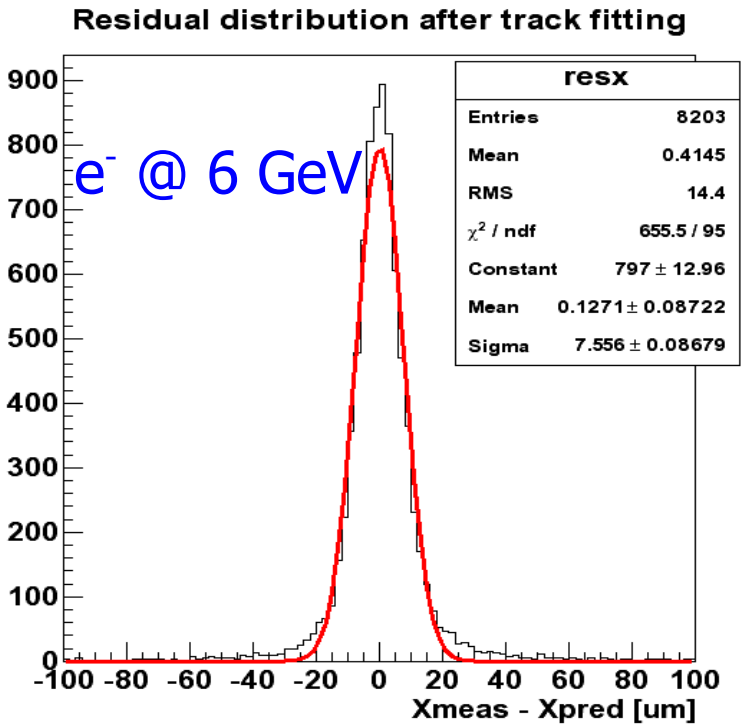




- Electrons up to 6 GeV
- 3 x-y planes silicon reference telescope
- Event rate ~Hz (MAPS + reference telescope)
- VME telescope readout + dedicated ADC board for MAPS
- Cooling to –15°C possible
- Dec '04 – Jan '05 run: 400000 events

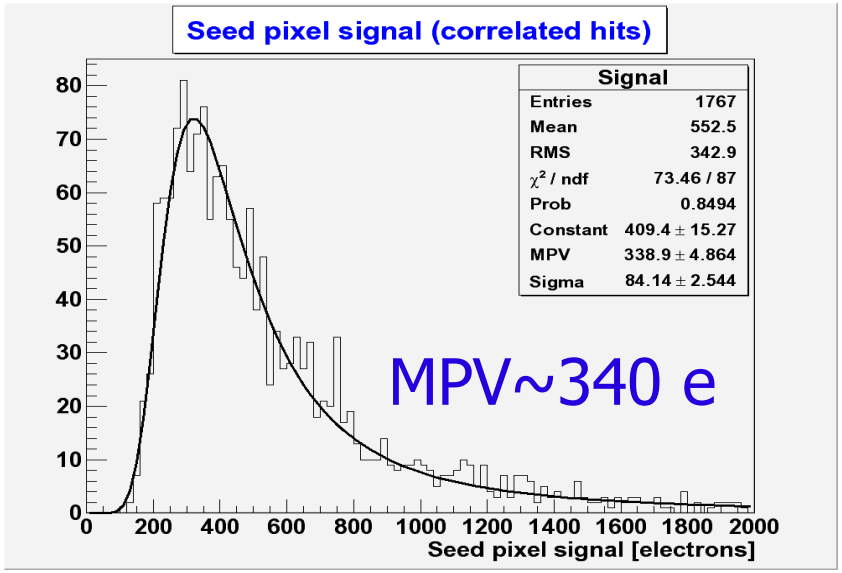
The silicon reference telescope

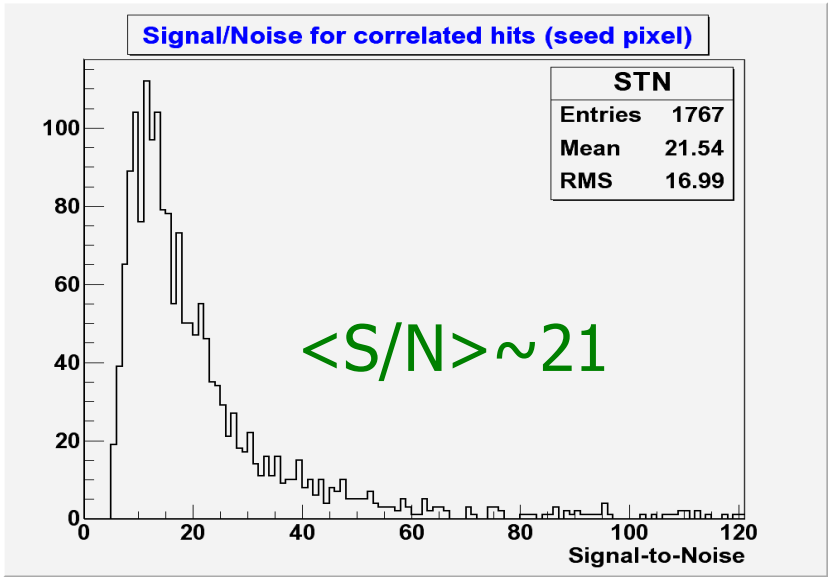




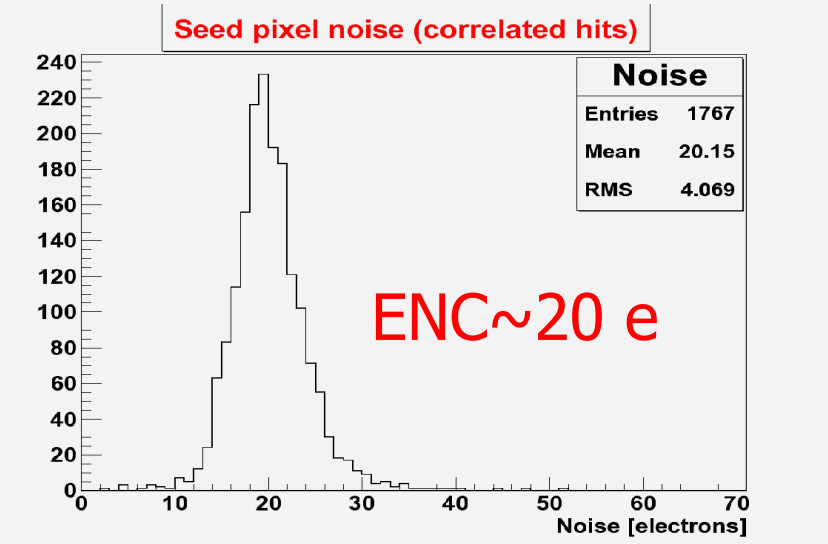
- Single-sided silicon microstrip detectors, 50 μm readout pitch
- Detection efficiency>99%, S/N~45-85
- Intrinsic resolution~3 μm, but in real life... multiple scattering!
- In this work: track fitting with ~6 μm precision

Beam-test results: signal & S/N

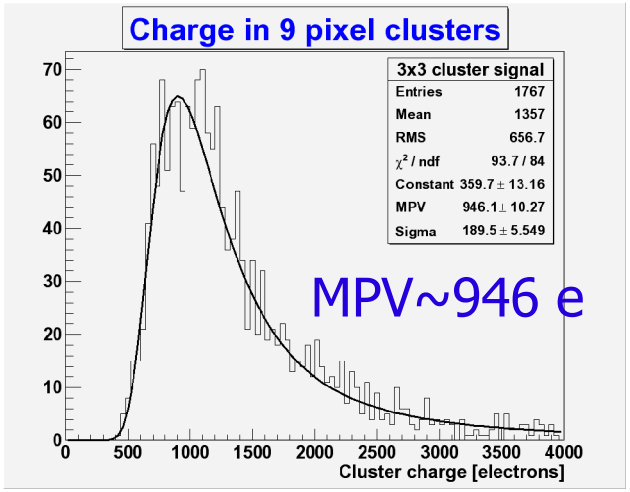


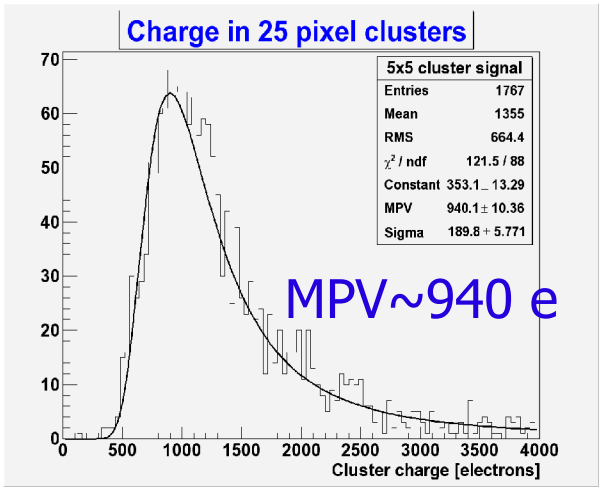


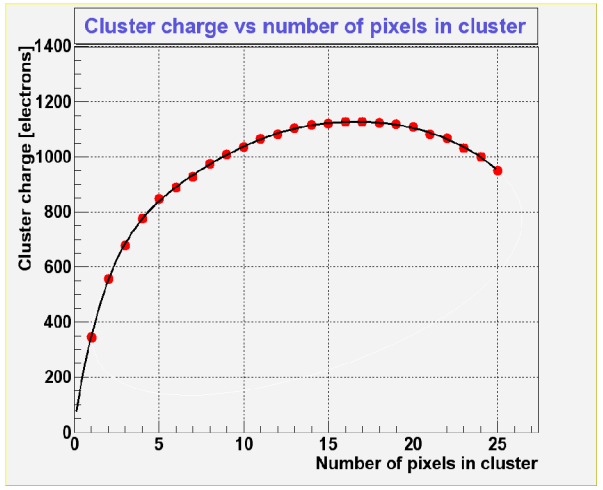
- 6 GeV electrons, cooling to -10°C
- Applied cuts: $S/N_{seed}>5$, $S/N_{neigh}>2$
- MPV for seed pixel signal ~340 e
- ENC~20 electrons
- Average Signal-to-Noise~21



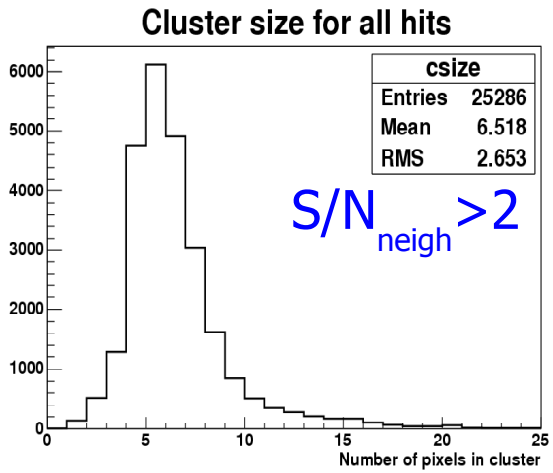
Beam-test results: cluster charge

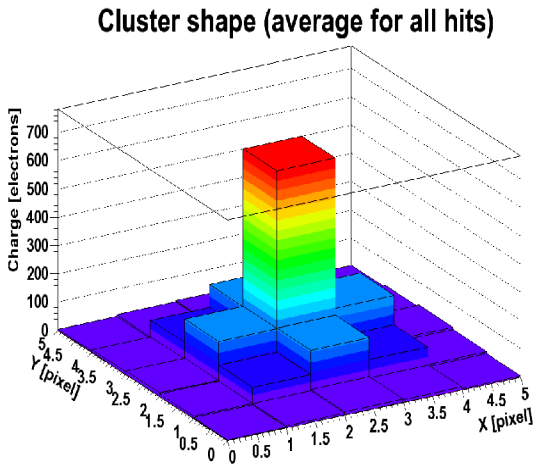






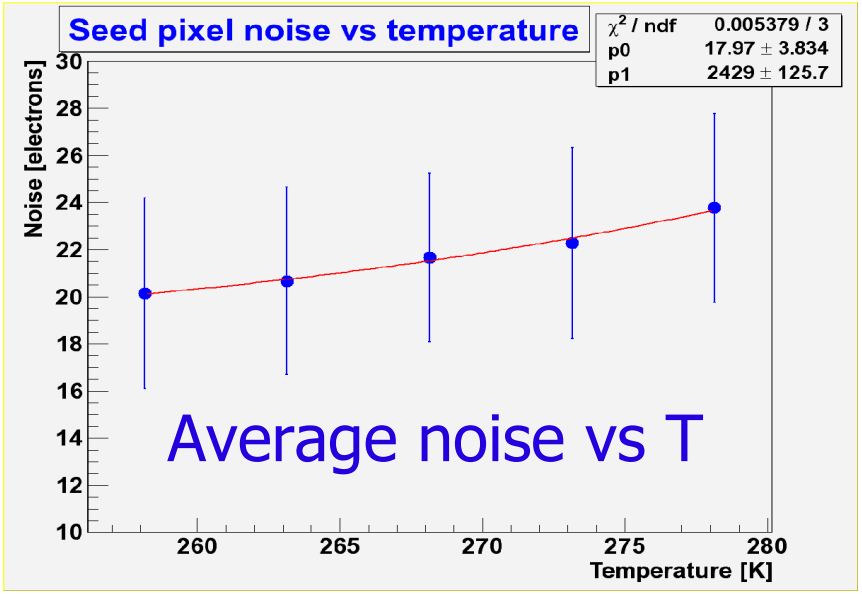
(pixel sorted by decreasing charge)

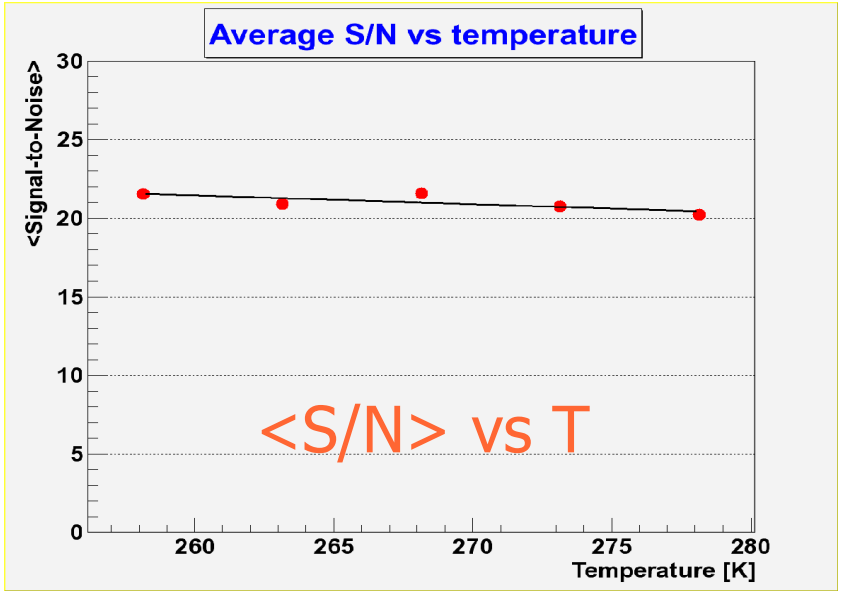




- Average cluster size ~6
- Most of the charge collected within 9 pixel
- Symmetric charge sharing

Signal-to-noise: temperature dependence





(bars= RMS of pixel distribution)

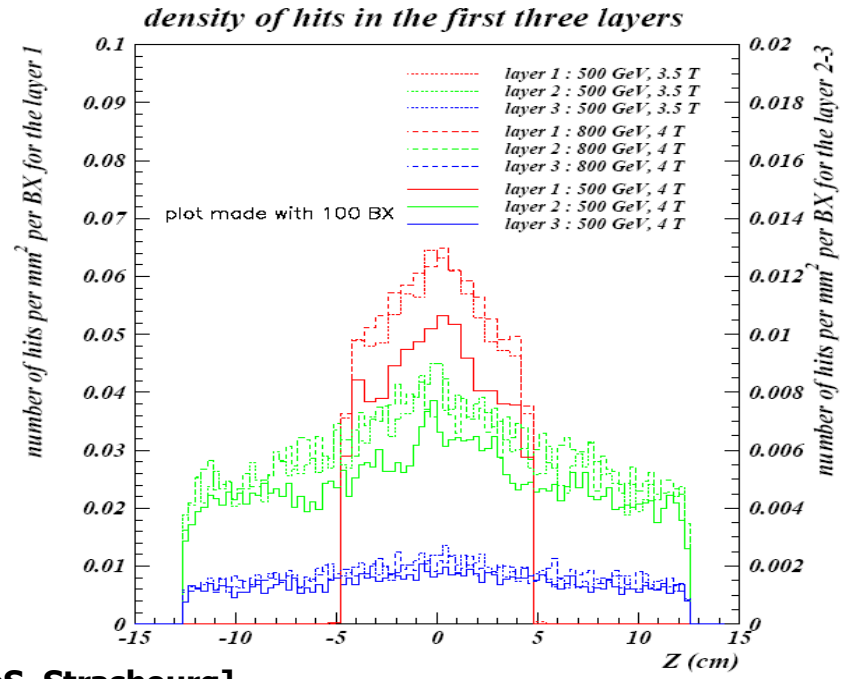
$$noise = c_0 + c_1 \sqrt{T^2 \exp(-\frac{E_g}{2k_B T})}$$

Leakage current term

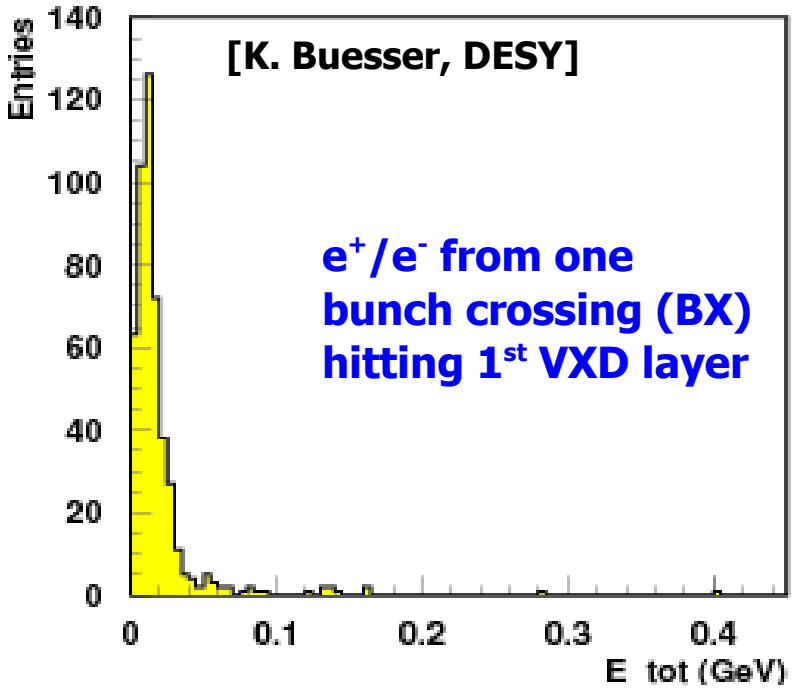
Noise $\propto (I_{leak})^{1/2}$

- Measurements performed from -15°C to +5°C
- Cooling is needed to keep noise level low w.r.t. room T
- Slight dependence of S/N between -15°C and +5°C

Electron background in the VXD

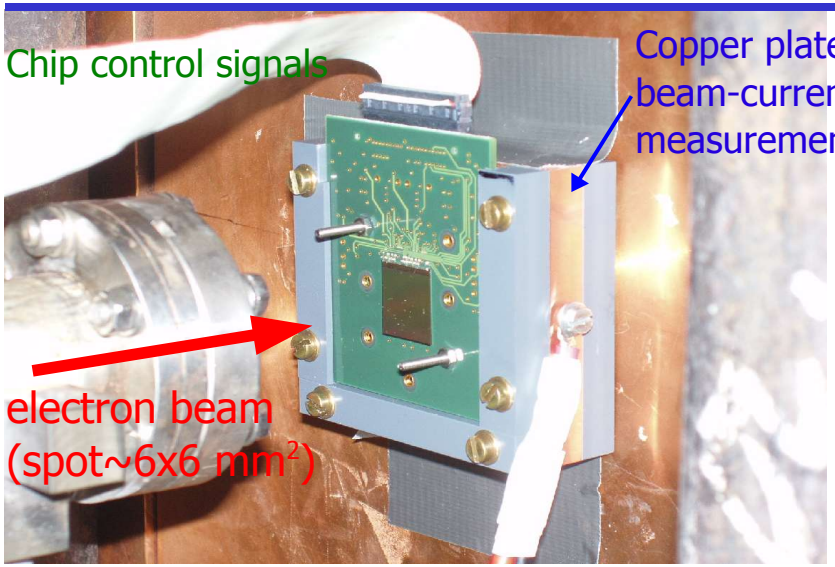


[©IReS, Strasbourg]



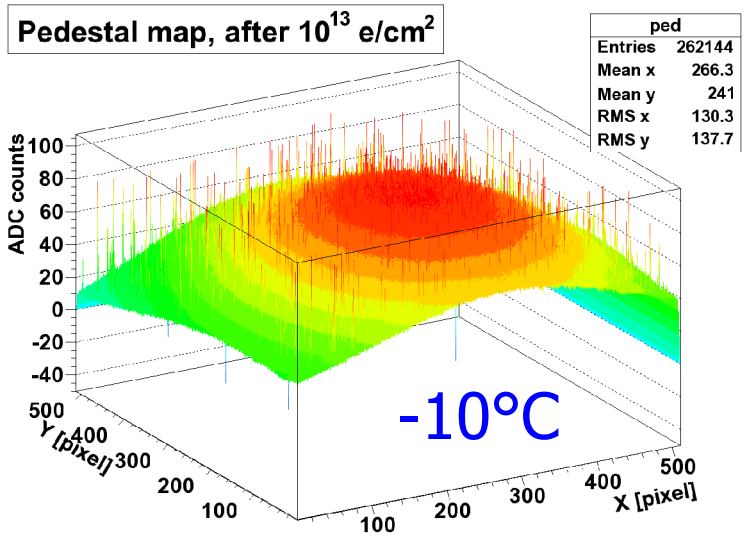
- Background of low momentum e^+/e^- from beamstrahlung
- For B_{field}=4 T, only e^+/e^- with p≥9 MeV/c reach first VXD layer
- At 90° ~5 hits/cm^2/BX expected → 6×10^{11} e/cm^2/year
- Necessity for radiation hardness assurance against ~10 MeV electrons

MIMOSA V irradiation with 10 MeV electrons

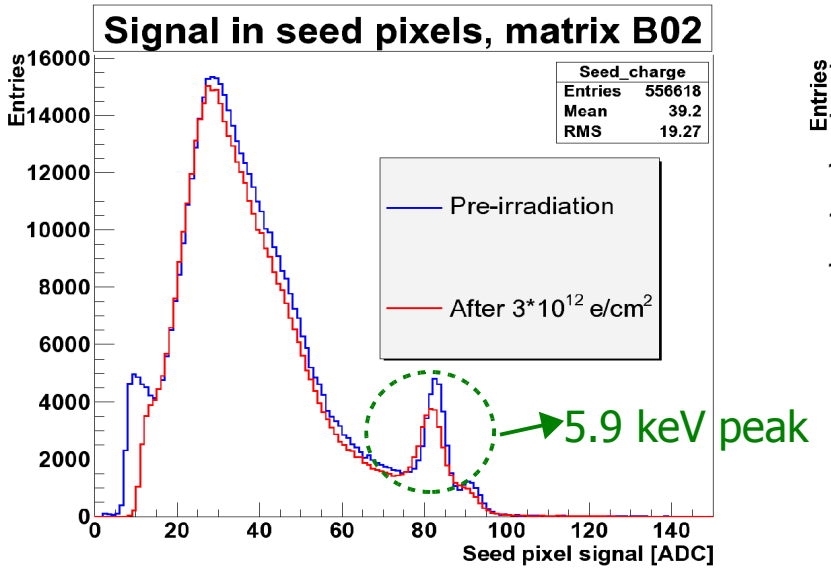


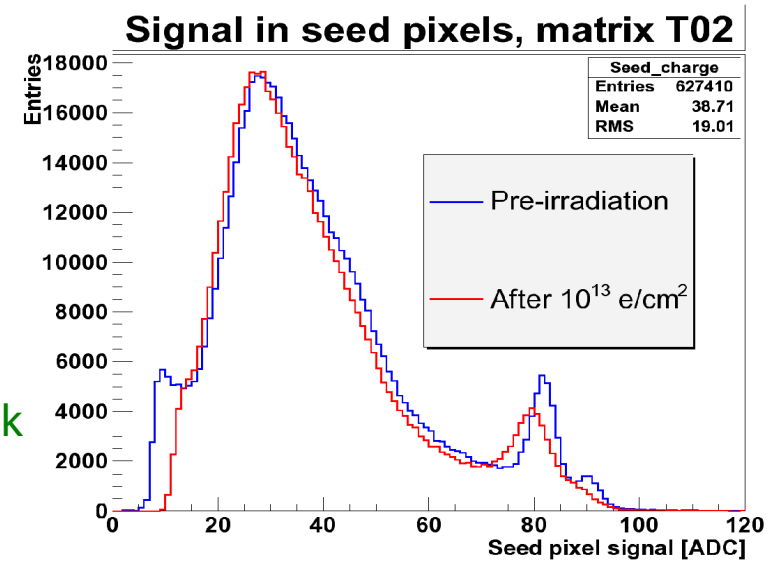
- Performed at the S-DALINAC of Darmstadt Technical University (Germany)
- 9.4 MeV electrons, current~1 nA
- Irradiation under bias & clock
- Fluences of 3×10^{12} and 1×10^{13} e/cm^2 (resp. 70 and 230 krad) on 2 different matrices

- After irradiation: need for cooling to retain detector operability
- Pedestal levels strongly and non-uniformly shifted (correlated with dose)

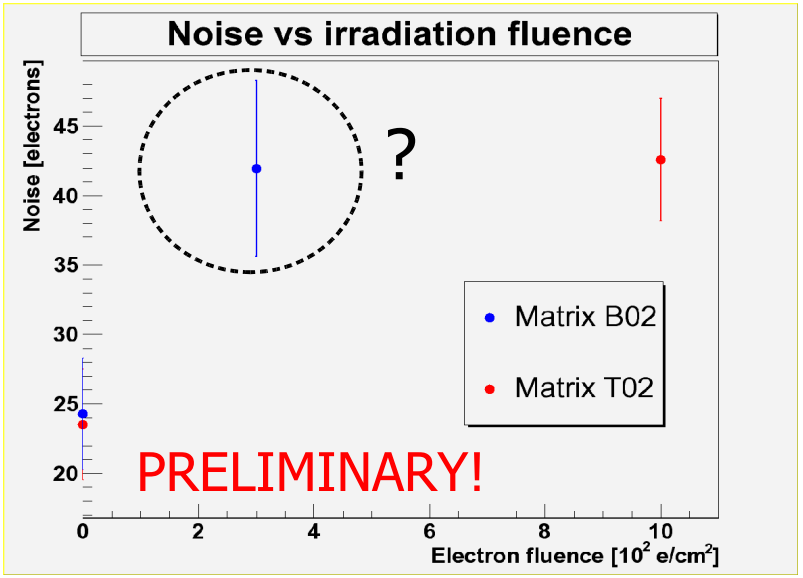


Preliminary results from ^{55}Fe calibration





- Measurements performed at -10°C
- Loss in performance observed from calibration characteristics
- Further studies under way



VXD cooling studies

Cooling requirements

- for complete pixel detector up to ~1kW of cooling needed if readout electronics stays on between bunch trains
- cooling should involve as little material in the tracking volume as possible

First attempt with gas cooling of whole detector volume: velocity of gas~30m/s needed, too high for light structure of ladders

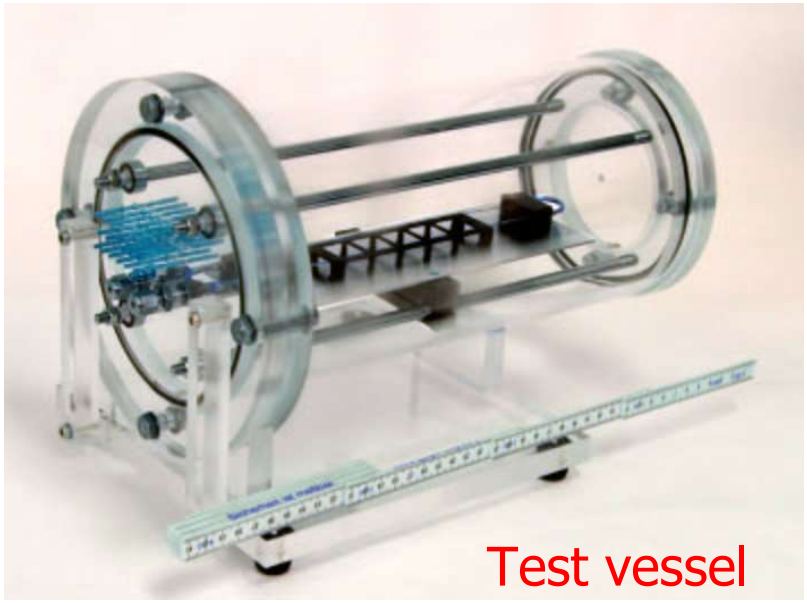
Present strategy

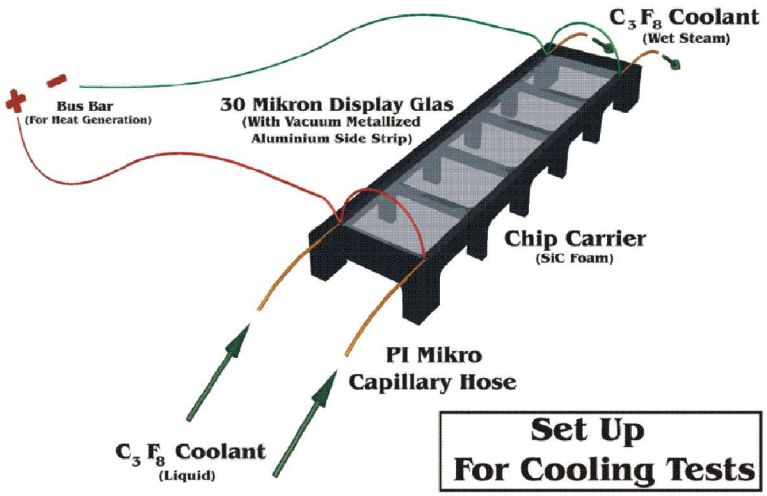
- system of cooling pipes in contact with ladders
- evaporative cooling: mixture of gas and fluid, evaporation heat used for cooling

Simulation of ladders

- instead of Si-ladders use 30 μm thick glass plate with thin Al-pattern to simulate mechanical properties and heat load

Setup for cooling tests





- evaporative cooling (like ATLAS) using octafluoropropane C_3F_8
- vessel with 30 µm glass ladders (SiC foam support) and aluminum strips to simulate power dissipation, 300 µm capillaries for cooling liquid
- tests under way

(J. Hauschildt, DESY)

Issues for future developments

Read-out architecture/speed

- Optimization to different VXD layers requirements
- First VXD layers: need for fast readout and signal processing

- CDS on-pixel + column-parallel readout

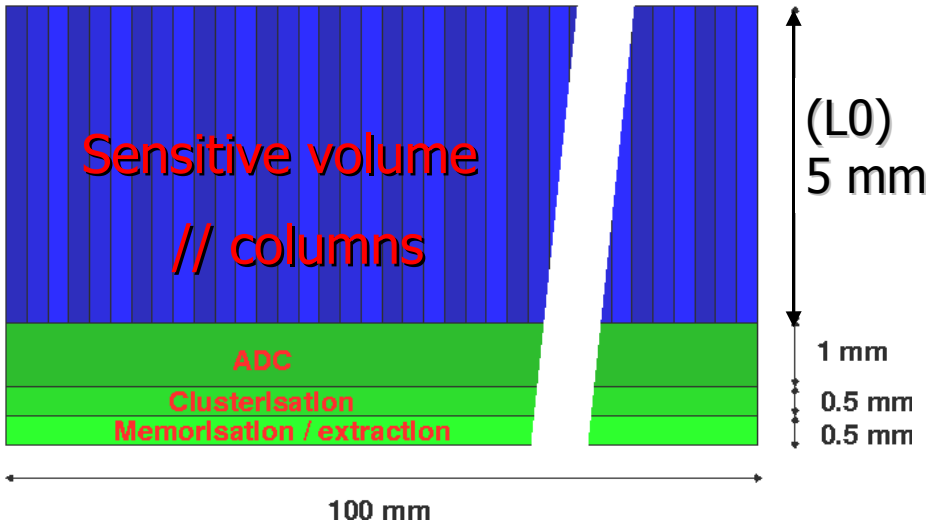
- ADC + signal processing and extraction at end of column

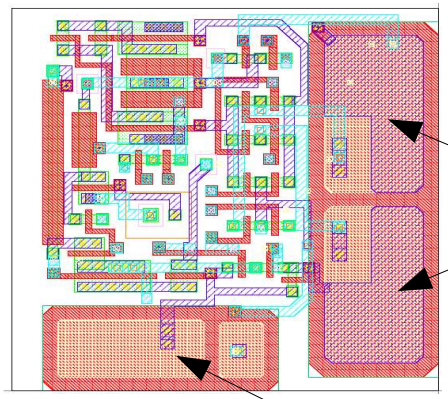
- Outer layers: lower rate but larger data flux

- on-pixel charge storage (multi-capacitors, larger pixel size)

- signal processing between bunch trains

- Several prototypes fabricated to study different features





MIMOSA 6 pixel layout

Charge storage capacitors

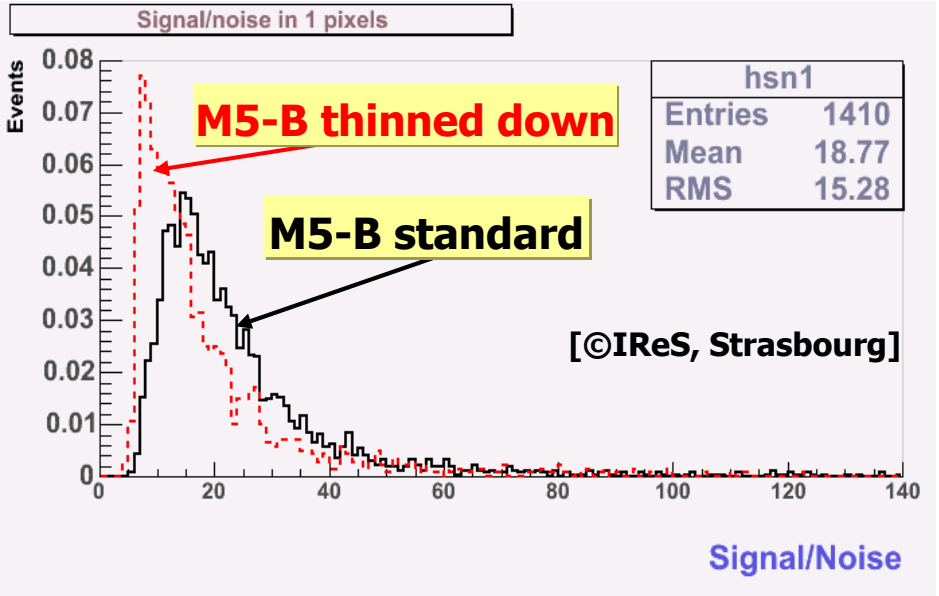
AC coupling capacitor

[M. Winter, talk@LCWS05]

Issues for future developments (2)

Thinning

- Real-size sensor thinned to 15 μm (substrate removal) operative but loss of performance observed
- Goal: thinning to 25-50 um



... and many other issues:

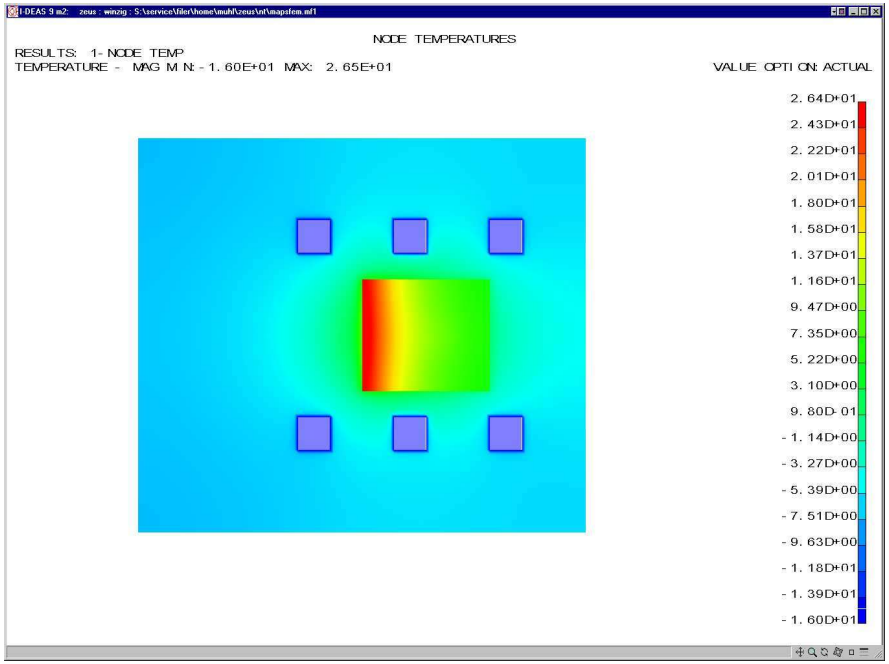
- Prototype ladder fabrication: interconnection, routing of the lines, handling
- Radiation hardness assurance against low energy e^+/e^- background
- Power pulsing tests
- Exploration of different fabrication technologies (<0.25 μm) and pixel architectures

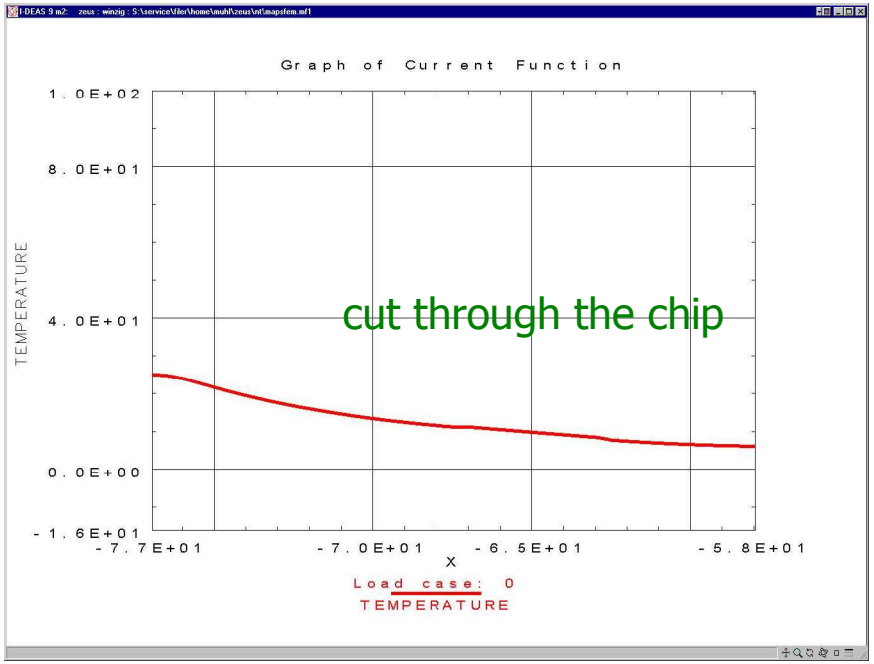
Summary and Conclusions

- Monolithic Active Pixel Sensors show excellent performances for particle tracking and are a promising candidate for application in the VXD at the ILC
- DESY/Uni-Hamburg group active on chip tests, radiation studies, physics simulation and engineering issues
- Our achievements (covered in this seminar):
  - development of detector simulation tools: charge collection simulations
  - large-scale prototype (~1 Mpixel) tested with radioactive sources and electron beam
  - cooling studies: simulation and test of power dissipation
- Several issues for future developments... much room for work!

SPARE SLIDES

Simulation of temperature distribution

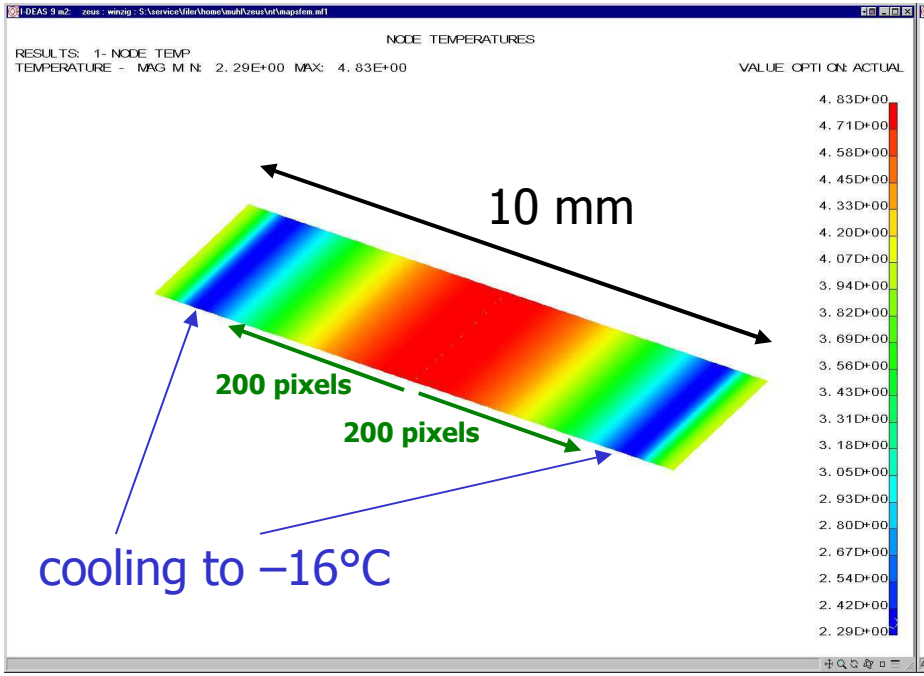


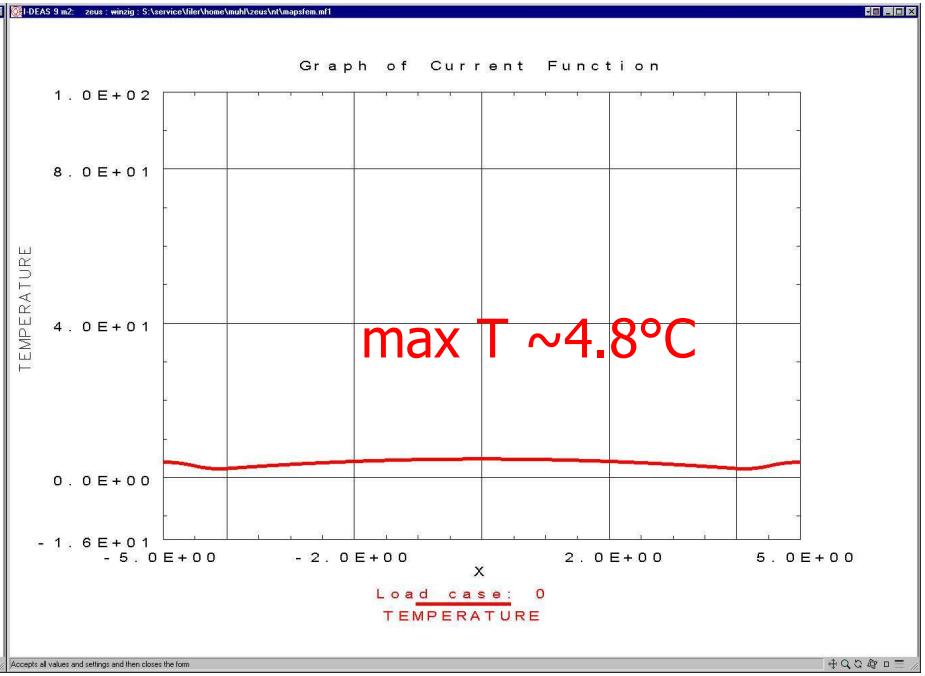


- simulation of cooling conditions in our experimental set-up
- Mimosa 5 chip in a brass box cooled down to -16°C, nitrogen flow
- Chip thickness 120 µm, PCB board modelled with a 0.035 mm copper layer
- Convective heat transfer coefficient $\alpha \sim 10$ W/m^2·K
- Temperature distribution simulated with I-DEAS®-TMG®
- Chip temperature varies from +26°C in the readout area to +6°C in the pixel area

(C. Muhl, DESY)

Simulation for central VXD ladder

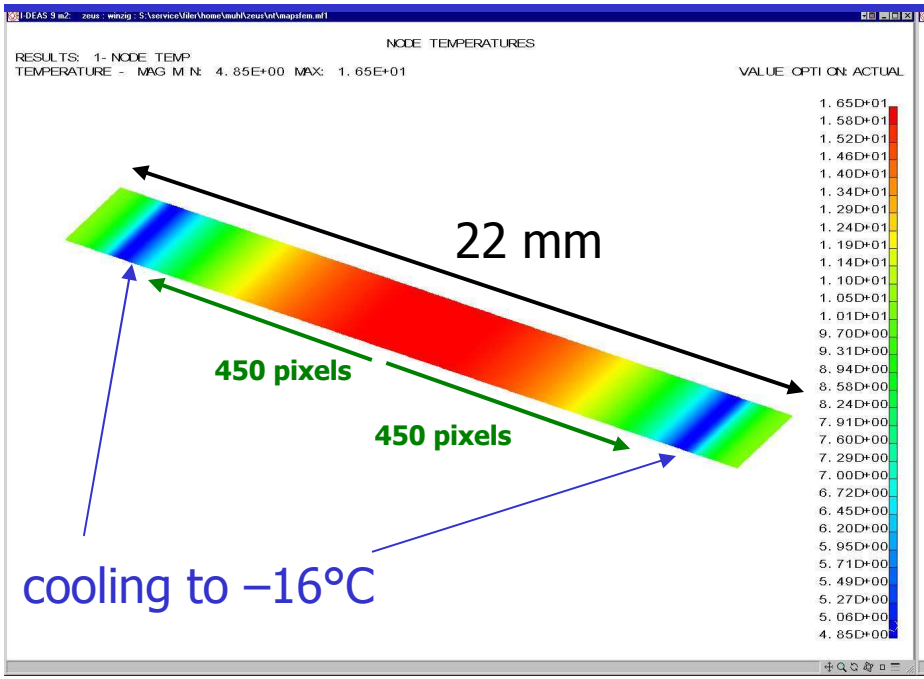


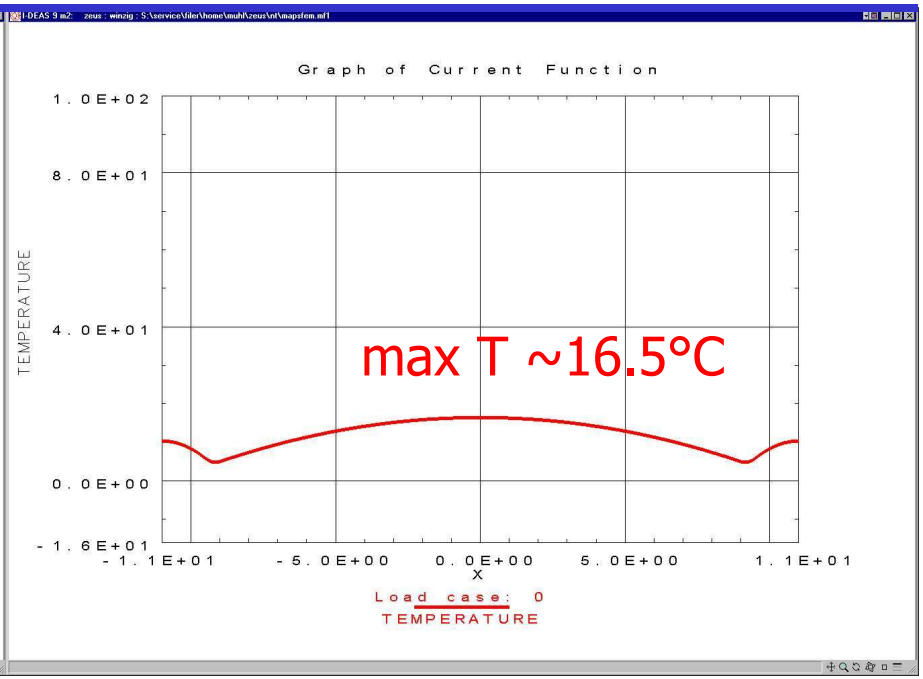


- 3 mm long portion of 10 mm wide ladder, 30 μm thick
- Thermal coupling: 2500 W/m^{2}K to a –16°C fluid, via two 0.5 mm wide strips on both sides of the bottom (a better coupling is feasible)
- No convective coupling to environment gas
- Under these conditions cooling is much better than for a single chip

(C. Muhl, DESY)

Simulation for outer VXD ladder





- 3 mm long portion of 22 mm wide ladder, 30 μm thick
- Thermal coupling: 2500 W/m^{2}K to a –16°C fluid, via two 0.5 mm wide strips on both sides of the bottom (a better coupling is feasible)
- No convective coupling to environment gas
- Higher maximum temperature than for central ladder

(C. Muhl, DESY)